Freescale Semiconductor
Design Workbook

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COM Express Carrier Development System Design Workbook

This document primarily describes the COM Express carrier board, its relationship to the whole COM Express development system, and the differences between the carrier board's architected functions depending on the processor module in use.

The COM Express carrier development system, referred to in this document as COMExprsDS, is a high-performance, computing, evaluation, and development platform supporting a single-board computing (SBC) COM Express module based on Power Architecture® processor.

The COM Express carrier board is a lead-free, RoHS-compliant board that supports various COMe processor module types. Each COMe processor module (hereafter referred to as COMe module) includes a primary processor or one of its derivatives, and Figure 1 shows how the various modules plug into the common carrier board.

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Table 1 shows the processors currently supported by each COMe module type and the orderable part number for each kit.

Table 1. Supported Processors and Kit Ordering Information

COMe Module Type	Processor	Kit Part Number
COMe1	P4080	P4080COMe-DS-PB
COMe2	P2020	P2020COMe-DS-PB

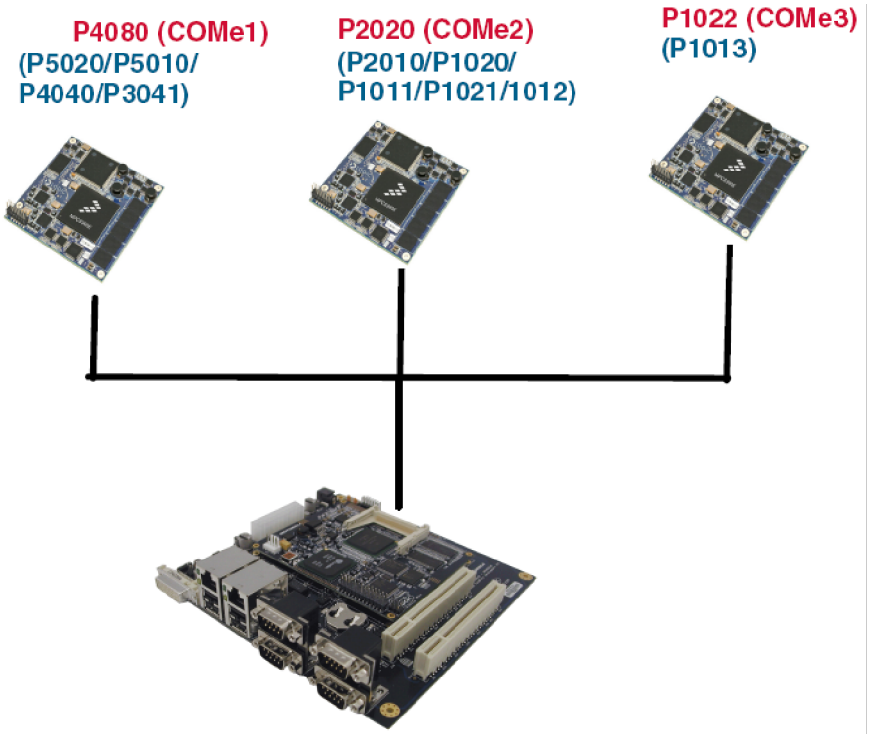


Figure 1. How Various Module Types Fit into the Common Carrier Board

NOTE

In the future, the COM Express carrier board will support the P5020/P5010, P4040, P3041, P2010, P1021, P1020, P1011, P1012, and P1013 devices.

Having a common carrier architecture that supports all of these devices as plug-in modules saves development time and money, because many devices can be evaluated with only a single investment in the remaining components of the development system; the peripheral IO modules, chassis, and power supply remain unchanged.

The COMExprsDS feature set is determined primarily by the type of COMe module in use and then by the actual processor on the module. Based on this feature set, the development system provides typical OS-dependent resources (disk, Ethernet, and so on) for that configuration. Therefore, this document describes the general development system features first, followed by the COMe module type features, and then the processor device specifics and how they are used by the carrier board.

1 COMExprsDS Features and Architecture

The general features of the COMExprsDS are as follows:

- Carrier/COMe connectors and supported functions that include the following:
  - — Standard ATX power supply connector
  - — One SD card/MMC connector
  - — Two dual CAN connectors
  - — SerDes PCI-Express (PCIe) connector
    - – Five PCIe x4 connectors (connector “A” through connector “F”), which can support up to four lanes of PCIe 2.0/1.0, SGMII, sRIO, and XAUI, depending on what processor is used
    - – Two PCIe x1 connectors (used as sideband connectors for the PCIe x4 connectors) and one PCIe x1 connector used for a TDM riser to support SLIC functionality
  - — Eight USB2.0 connectors
  - — Four SATA II connectors
  - — One DVI-I connector to support either analog VGA (via an adapter) or digital DVI connector
  - — LVDS A and B ports to support two, single-link DFP (TFT panel) displays with optional LVDS panel and touchscreen functionality
  - — Two UART DB-9 RS-232 connectors (UART0/1 serial ports) that operate at up to 115200 Kbps
  - — One stereo audio jack
  - — Three gigabit Ethernet ports 0/1/3 supporting one dual and one single GMII (1-GHz) RJ-45 Ethernet connectors
    - – One dual-port PHY supporting one dual RMII (100/10-MHz) connector for COMe2 (only for processors that feature QUICC Engine (QE) functionality).
  - — IXXAT
    - – 50-pin connector for Industrial Ethernet Module via SPI bus
  - — Tamper detect circuitry to test out P5020/P3040 security modes
  - — SLIC
    - – RJ-11 phone connectors can be added by using a TDM riser card into slot 5 and the TDM riser sideband connector
  - — RS-485 can be added by adding an adapter to the DB-9 RS-232 connector.
- Multifunction FPGA
  - — Routes low-speed and user-defined signals from the COMe module board connectors to the appropriate connectors and devices located on the COM Express carrier board.
  - — Programmed by the processor on the COMe module following a power-up or hard reset. The FPGA functionality varies depending on the specific processor populated on the COMe module.
  - — Generally interfaces to the following signal groups on the COMe module connectors:
    - – Reserved/user-defined
    - – UART2 and UART3

  - TDM
  - SSI
  - GPI
  - GPO
- Interfaces to the following connectors and devices on the COM Express carrier board for processors that feature QUICC Engine (QE) functionality:
  - Two RS-232 serial ports with corresponding DB9 connectors (UART 2/3)
  - Two RS-485 serial ports with corresponding DB9 connectors
  - Four CAN ports with corresponding connectors
  - UTOPIA module and connector using Freescale PQ-MDS-QOC3 card
  - HDLC module and connector using Freescale PQ-MDS-16T1E1 card
  - TDM-based SLIC modules
  - Fast Ethernet PHY (RMII/MII)
  - SSI-based CODECs
  - 1588 header—support is TBD

- Other functions routed from the COMe module to carrier board devices are:
  - Local bus
    - 128-Mbyte NOR FLASH on COMe1 module for Freescale debug purposes only
  - eSDHC
    - Connects to SDMedia card slot for boot code or mass storage
  - SPI
    - 16-Mbyte EEPROM module for boot code and storage
    - Control interface for LVDS touchscreen
  - I^2C
    - Three I^2C controllers from COMe module
    - One I^2C2 master implemented in FPGA to read I^2C2 EEPROM to determine processor type
    - I^2C1 to I^2C expander to generate eight GPIOs (five to FPGA, three to IXXAT module)
    - I^2C2 to control LVDS interface and FPGA I^2C2 slave mux/demux for COMe2 (P1021/P1012 only)
    - I^2C3 to control DVI/VGA interface and FPGA I^2C3 slave mux/demux for COMe2 (P1021/P1012 only)
  - Debug features
    - Legacy COP/JTAG and USBTAP headers for use with CodeWarrior software
- System logic CPLD and FPGA—other functions
  - CPLD manages power sequencing
  - Enabling/disabling of functions based on processor type
  - Mux/demux functions for QE functions, based on I^2C2 or I^2C3 slave register settings
  - I^2C1 master reads processor type

- Clocks
  - SerDes clock
    - Two clock buffers
    - Sd_refclk1 pair supports PCIe, and sd_refclk2_p/n supports SGMII and XAUI
- Power supplies
  - Power is supplied to carrier board via standard ATX power supply
  - Power is supplied to COMe module via +12 V pins, VCC_RTC=3.3 V, and VCC_5V_stby = 5 V on the COM Express connectors
  - 2.5-V power for RMII Ethernet PHY

1.1 COMExprsDS as a Processor Evaluation System

For general hardware and/or software development and evaluation purposes, the COMExpress development system can be used like an ordinary, desktop computer.

The P4080COMe-DS-PB and P2020COMe-DS-PB development systems can also be used to evaluate many features of the P4080 and P2020 processors, respectively. Table 2 summarizes the processor hardware interfaces that can be evaluated by using the COM Express carrier board; note that shaded features apply to only one processor.

Table 2. COMExprsDS Device Interfaces

Device Feature	Configuration Options
SerDes	• Connect to PCI Express slots for use with graphics or other PEX cards • Test via PCI Express card (typically graphics) or Catalyst™ PCI Express control/monitoring card
LVDS	Use ports A or B to test single-link DFP using LVDS TFT LCD panel and touch screen for applicable modules
eSDHC	For P2020 only: Supports SDMedia cards and MMC cards
SPI	Supports standard and x4 devices
Local bus	For P4080 only: Internal debug
Serial	UART supports two 4-wire serial ports
I^2C	I^2C bus #1 can be used for the following: • Boot initialization code • System EEPROM (MAC address storage, serial number, and so on) • Processor EEPROM for COMe module and processor ID from I^2C master in the carrier FPGA • Expander to interface to I^2C slave in the carrier FPGA (TBD)
	I^2C bus #2 can be used for the following: • RTC on the COMe module • interface to LVDS control
	I^2C bus #3 can be used for the following: • interface to VGA control
Clocking	• SerDes clock buffers for XAUI/SGMII/Serial RapidIO and PCI Express slots • RMII clock and buffers
GPIO	Eight GPIOs come from I^2C expander

Table 2. COMExprsDS Device Interfaces (continued)

Device Feature	Configuration Options
IRQs	EVENT switch normally asserts IRQ* but can drive SRESET0, and/or SRESET1 via software setting
Power	ATX power supply to COMExpress connector VCC_12, VCC_5_STBY, VCC_RTC_BAT

1.1.1 Development System Use

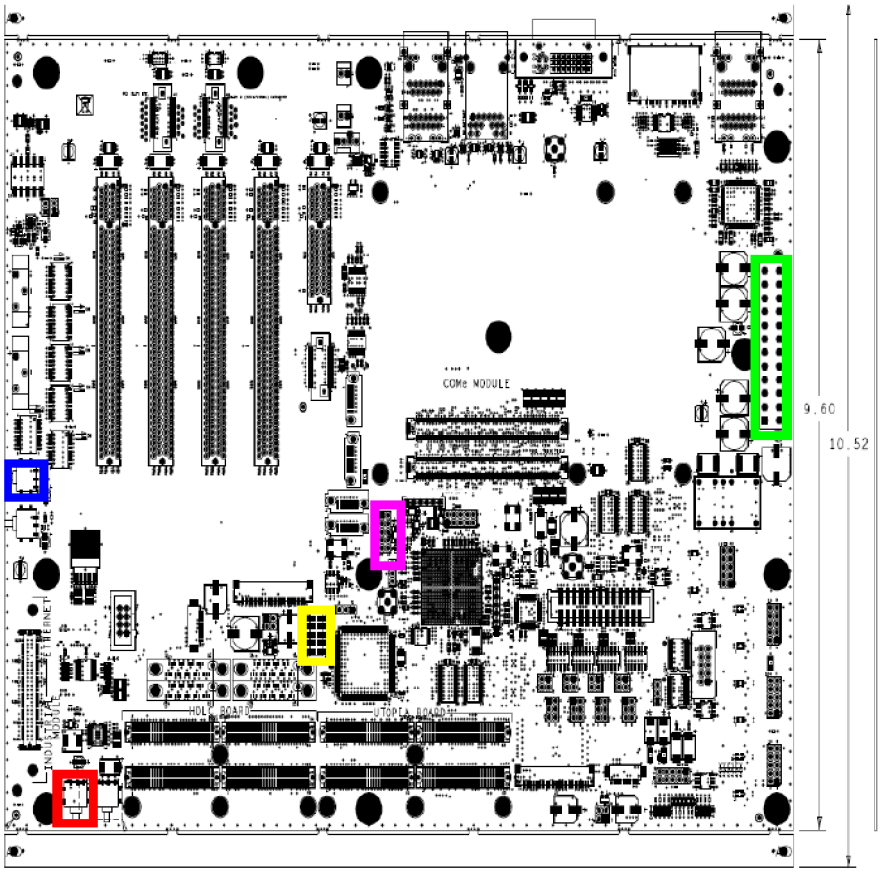
In the absence of special hardware or software configuration, the COMExpress development system operates identically to a development/evaluation system such as ArgoNavis (8641DS) or other members of the HPC family.

1.1.2 Embedded Use

Section 2.2, “Carrier Board Configuration Switches When Used with a P4080 COMe1 Module,” and Section 3.2, “Carrier Board Configuration Switches in a System with a P2020 COMe2 Module,” provides the FPGA and external configuration switch settings used for start up configuration information for U-Boot or Linux when the system is used as an embedded platform.

1.2 Difficult-to-Find COMe Carrier Connections

Figure 2 highlights connections that are difficult to find on the COM Express carrier board.



Key:
ATX power connector
SW3 power-on button
SW1 local reset
CPLD programming header
FPGA programming header

Figure 2. Difficult-to-Find Connections—COM Express Carrier Top View

1.3 System Logic (CPLD and FPGA) Architecture and Functionality

The carrier board contains a CPLD used for power sequencing, and an FPGA that implements the following functions:

- Transfers switch settings to processor/board configuration signals
- Performs reset sequencing
- Enables/disables functions based on processor type
- Implements miscellaneous system logic:
  — I^2C timeout reset-TBD

The CPLD is implemented with a MAX II, and the FPGA is implemented in an Altera Cyclone III EP3C16F484C8 in a 484-256-pad micro-BGA.

Figure 3 shows the overall FPGA architecture.

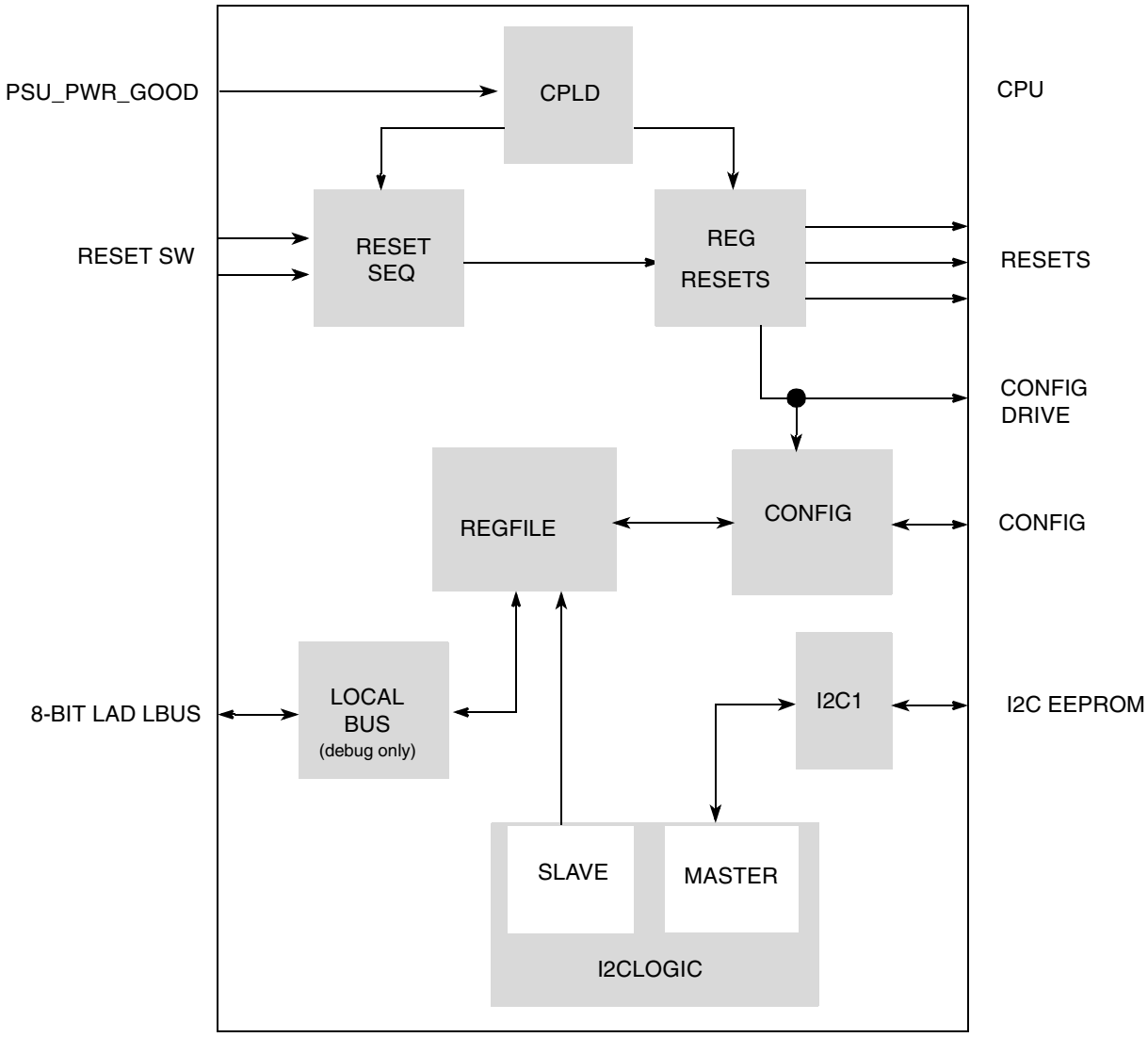


Figure 3. CPLD and FPGA Overview

Table 3 describes the various FPGA modules.

Table 3. FPGA Module Descriptions

FPGA Modules	Function
RESETSEQ	Collects various reset/power-good signals and starts the global reset sequencer[1, 2]
REGRESETS	Copies reset signals from the sequencer, but also allows register-based software to individually asserted reset to the local bus, memory, and/or compact FLASH interfaces.
REGFILE	A multi-ported register file containing status and configuration data[3]
LOCALBUS	Interface between the processor and REGFILE for internal Freescale debug use only[4]
CONFIG	Monitors and/or sets selected configuration signals[5]
I2CLOGIC and I2C1	The I2C1 master reads COMe module EEPROM at address 0xA8 to detect processor type and id information. An I2C slave is also used to select muxes for QE functions via the I2C1 expander FPGA_IO signals (first availability is for P1021 COMe2 module).
Power	Power for FPGA is supplied from dedicated VCC_HOT_3.3 and VCC_HOT_1.5-V power supplies based upon the ATX power supply +5-V standby power, VCC5STDBY.

1 ASLEEP indicates that the processors(s) have exited the reset state. It does not cause a reset, because the processor can sleep for any number of reasons after hard reset is completed.

2 During power-down, all I/O and output drivers are tristated. After power up, drivers may be driven. Normal operation and/or use of the VELA engine may cause some I/Os to be tristated.

3 REGFILE must be able to accept (or arbitrate for) concurrent writes to the same register, though this is not a statistically likely occurrence.

4 Because access to the internal registers may be blocked, asynchronous (not ready) signalling is used.

5 In some instances, CONFIG maps switch settings into direct configuration outputs, while in others (such as SYSCLK), it maps a 3-position switch into a 16-bit register initialization pattern, which is subsequently used to initialize the clock generator.

1.4 System Power Connections Between Carrier Board and COMe Module

The 12-V, 5-V, and 3.3-V power requirements of the carrier board are met by the attached ATX-12V compatible power supply unit (PSU) of the COMExprsDS. 5 V and 3.3 V are connected to individual power planes in the COMExprsDS PCB stackup. The 12-V power from the standard ATX header is treated as separate from the ATX-12V power, which supplies a large amount of current and is referred to as “VCC_12V_BULK” to the COMe module. Other supplies include VCC_5VSTBY, and VCC_BAT.

Note that to support the FPGA standby operation, video cards, or other high-power-dissipation cards in the PCI Express slot, the PSU should support the following minimum specifications:

- Minimum 450 W overall, 500 W recommended
- One PCIE 12-V connector (TBD)
- PCIE 12 V supports a minimum of 150 W
- Minimum 5-V, 2-A standby current

All other power sources are also derived from the ATX PSU. Figure 4 shows the principal system power connections in relationship to the CPLD control. For more detail about the processor power scheme implemented by this system, see “Power” in Table 3.

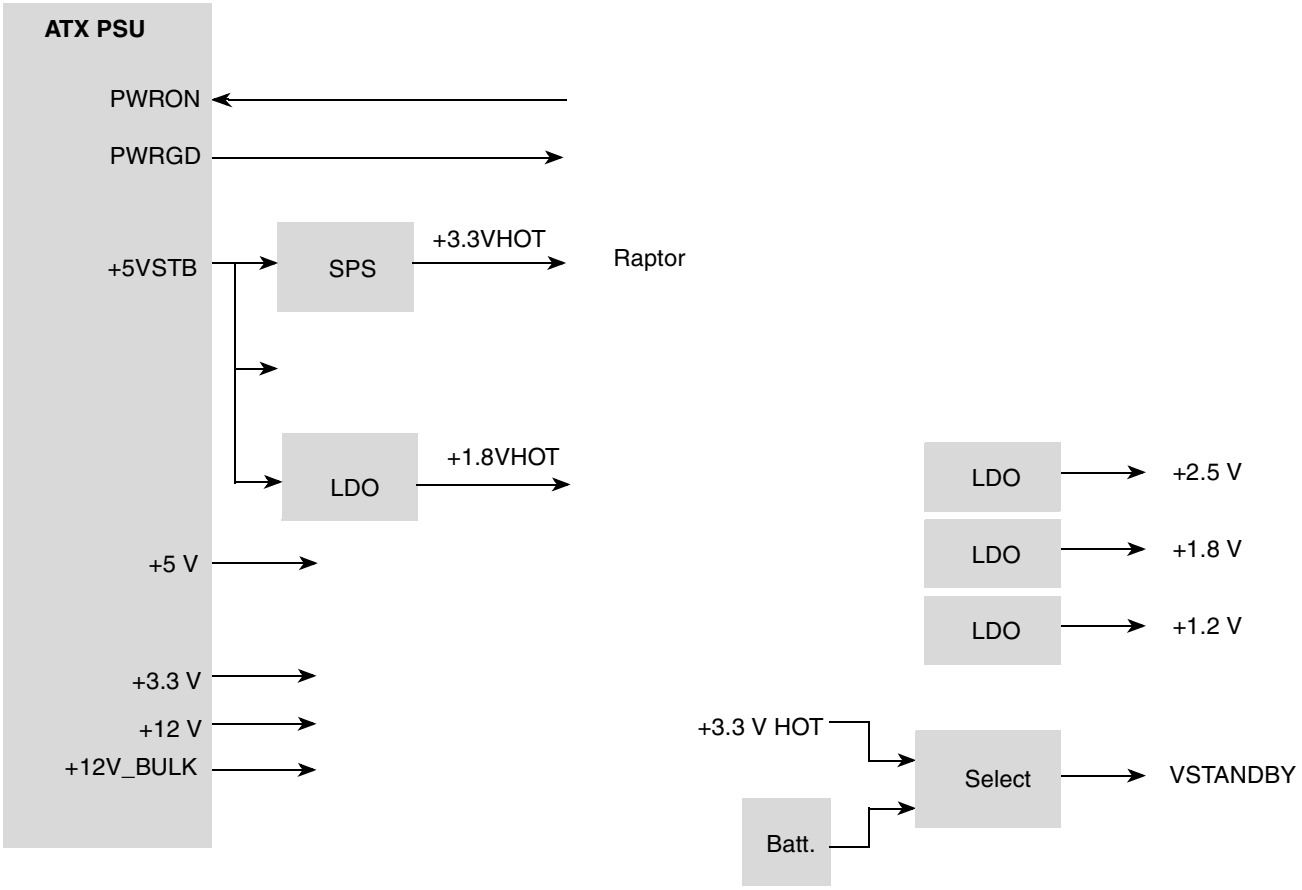


Figure 4. COMExprsDS System Power Supplies

2 COM Express Carrier Architecture When Used with COMe1-Type Module

As described earlier, the architecture and feature set of the carrier board depends on the module type with which it is used. Figure 5 depicts the general features and connectivity of the COM Express carrier board when used with a COMe1-type module board.

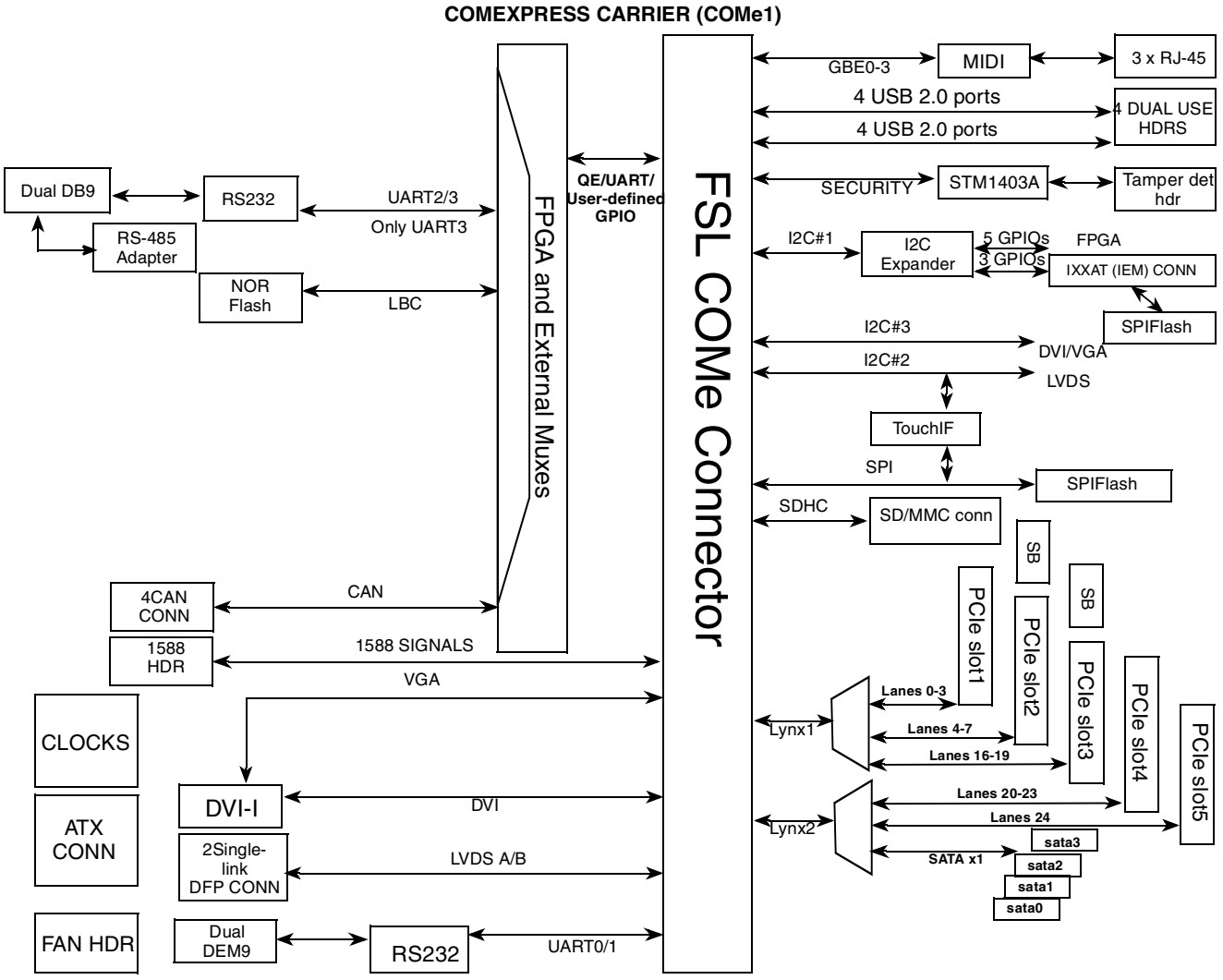


Figure 5. COM Express Carrier Block Diagram When Used with COMe 1-Type Module

2.1 System Reset Performed by FPGA Reset Sequencer in a System with a COMe1 Module

The carrier board FPGA contains a reset sequencer that properly manages the orderly bring-up of the system (this is not the same as the power sequencer, which is similar, but not specifically related to reset).

After the system transitions to having fully stable power supplies, the reset sequencer does the following:

1. Waits for all reset conditions to clear
2. Configures and releases the processor from reset
3. Idles waiting for further reset conditions to occur

Table 4 summarizes the reset conditions and actions of the FPGA when used with a COMe1 module.

Table 4. Reset Conditions and Actions of FPGA Reset Sequencer

Signal	Type	Description	Action
HOT_RST_B	External	HOT power stable	Restarts all FPGA internal state machines and registers
PWRGD	External	ATX power stable	Causes full system reset unless the system is in S3 (power down) state
SYS_HRST_B	External	COP tool reset request	Upon power good, sys_rst_b is sent from carrier to COMe1 module
RESET_REQ_B	External	CPU requests reset	Full reset

2.2 Carrier Board Configuration Switches When Used with a P4080 COMe1 Module

There are different types of carrier board configurations. A list of these configuration types and their implementation is shown in Table 5.

Table 5. Carrier Board Configuration Types

Configuration Type	Implementation
Requires software configuration to support evaluation	Implemented with “DIP switches” and/or software-settable options
Expected to be easily or often changed by the end-user or developer	

The carrier board switches and their default settings when used with a P4080 COMe module are shown in Figure 6. Switch names exactly match the name on the schematics and on the printed-circuit board in most cases, except where a spare has been newly assigned and only the FPGA has changed.

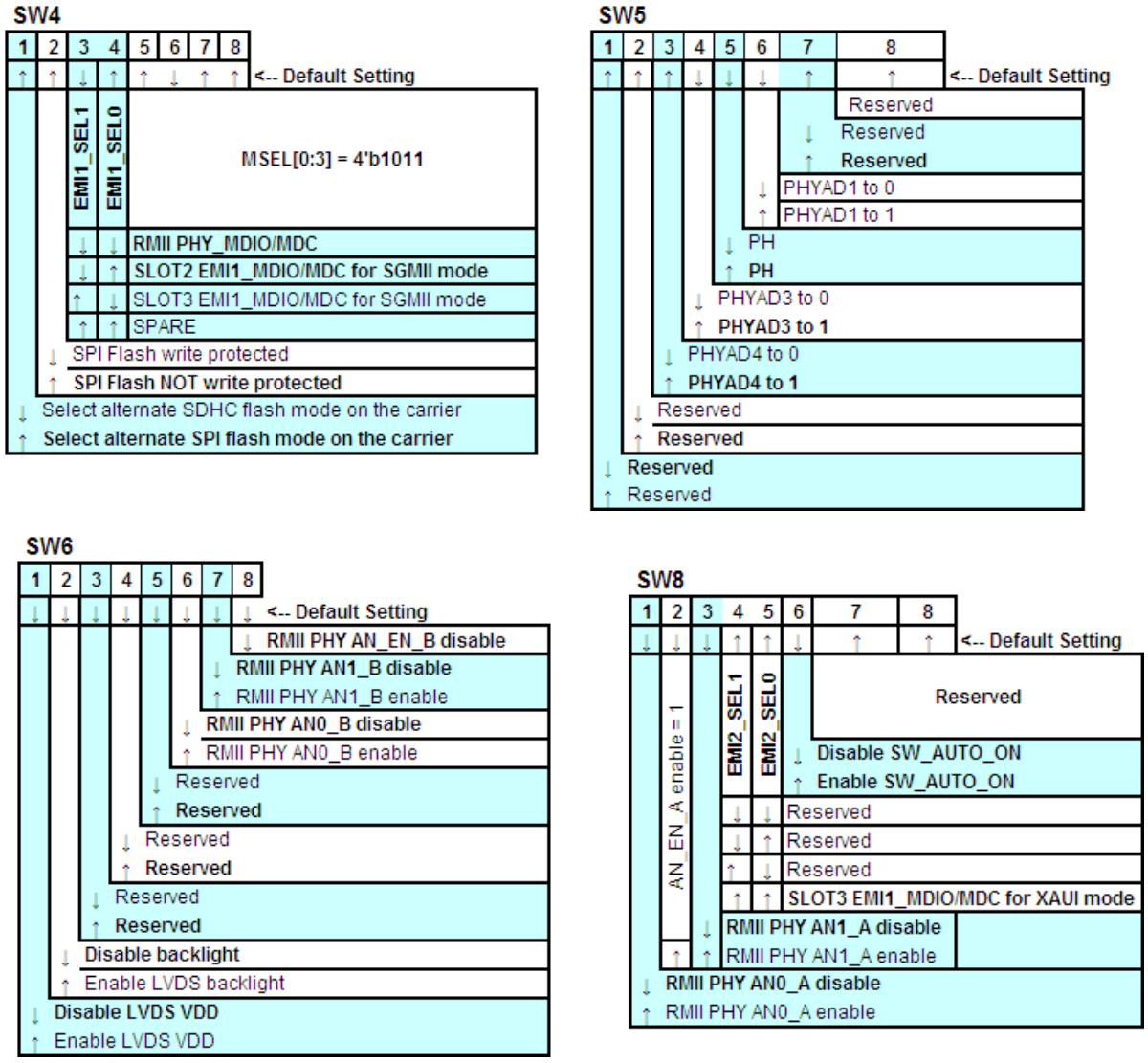


Figure 6. Carrier Board Switch Assignments and Defaults When Used with P4080 COMe Module

For those signals configured using switches, the configuration logic is as shown in Figure 7.

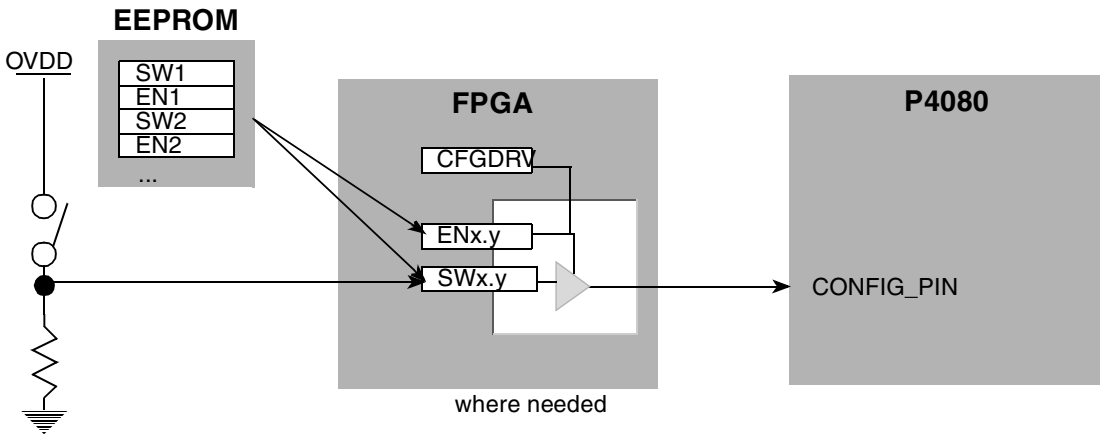


Figure 7. COMe1 Configuration Switch Logic and P4080

The default action is for the FPGA to transfer the switch setting to the processor configuration pin during the CB_RESET_B assertion interval.

For certain COMe modules, the I^2C expander FPGA IO signals can select the multiplexer configurations.

2.3 COM Express Carrier Board Functionality when Used with a P4080 COMe1 Module

The ways in which the COMe1 module affects the functionality of the carrier board also depends on the specific processor used in the COMe1 module. This section and its subsections are tailored to the carrier board functionality when used with the P4080 COMe1 module specifically.

Figure 8 shows the P4080 COMe module block diagram. Note that functional modules that only exist on the COMe module are described in the *COMX-P4080 COM Express Module* installation and user manual.

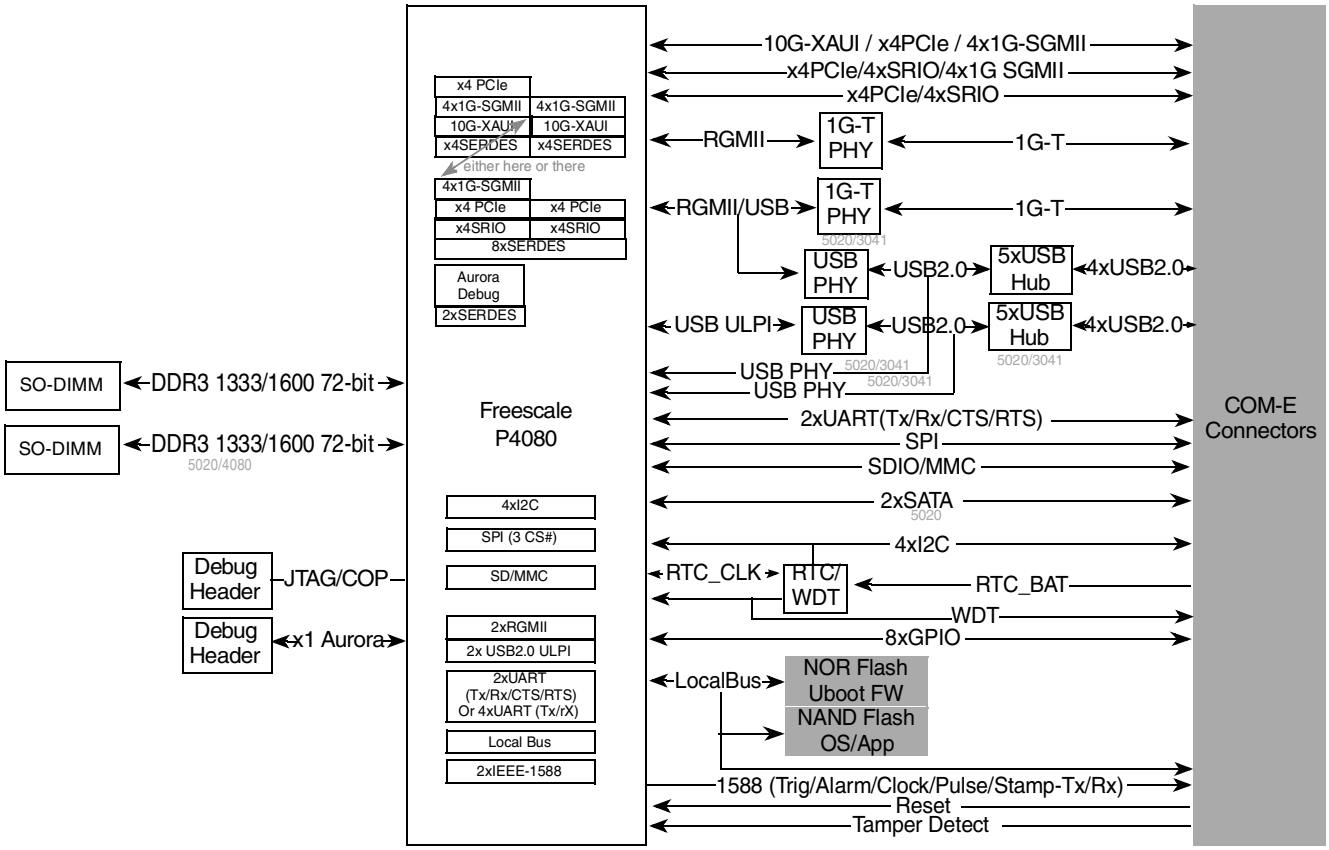


Figure 8. P4080 COMe Module Block Diagram

2.3.1 Carrier Board Use of P4080 DDR Interface

See the *COMX-P4080 COM Express Module* installation and user manual.

2.3.2 Carrier Board Use of P4080 SerDes x18 Interface

The SerDes block on the P4080 provides high-speed serial communications interfaces for several internal devices. The SerDes block on the P4080 COMe1 module provides 18 serial lanes for the carrier that may be partitioned as shown in Table 6.

Note that the term ‘lane’ is used to describe the minimum number of signals needed to create a bidirectional communications channel; in the case of PCI-Express or Serial RapidIO, a lane consists of two differential pairs, one for receive and one for transmit, or four in all.

Table 6, top down, shows the following clocking banks and how they are configured by the carrier board:

- Bank1—lanes A–D go to slot 1, E–H to slot 2, and I–J to the Aurora debug connector
- Bank2—lanes A–D go to slot 3
- Bank3—lanes A–B go to SATA ports 1 and 2

Table 6. P4080 SerDes Lane Multiplexing Configurations on Carrier

Bank 1										Bank 2				Bank 3			
A	B	C	D	E	F	G	H	I	J	A	B	C	D	A	B	C	D
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
SLOT 1				SLOT 2				Aurora Conn on COMe Module		SLOT 3				SATA Port1	SATA Port2	—	—
PCIe1 (5/2.5G)				PCIe2 (5/2.5G)				Debug (5/2.5G)		XAUI FM2				SATA1	SATA2	—	—
PCIe1 (5/2.5G)				SGMII FM2	SGMII FM2	SGMII FM2	SGMII FM2	Debug (5/2.5G)		XAUI FM2				SATA1	SATA2	—	—
sRIO2 (2.5G)				sRIO1 (2.5G)				Debug (5/2.5G)		XAUI FM2				SATA1	SATA2	—	—
sRIO2 (2.5G)				sRIO1 (2.5G)				Debug (2.5G)		SGMII FM2	SGMII FM2	SGMII FM2	SGMII FM2	SATA1	SATA2	—	—
sRIO2 (2.5G)				sRIO1 (2.5G)				Debug (5/2.5G)		PCIe3 (5/2.5G)				SATA1	SATA2	—	—
PCIe1 (5/2.5G)				sRIO1 (2.5G)				Debug (5/2.5G)		XAUI FM2				SATA1	SATA2	—	—

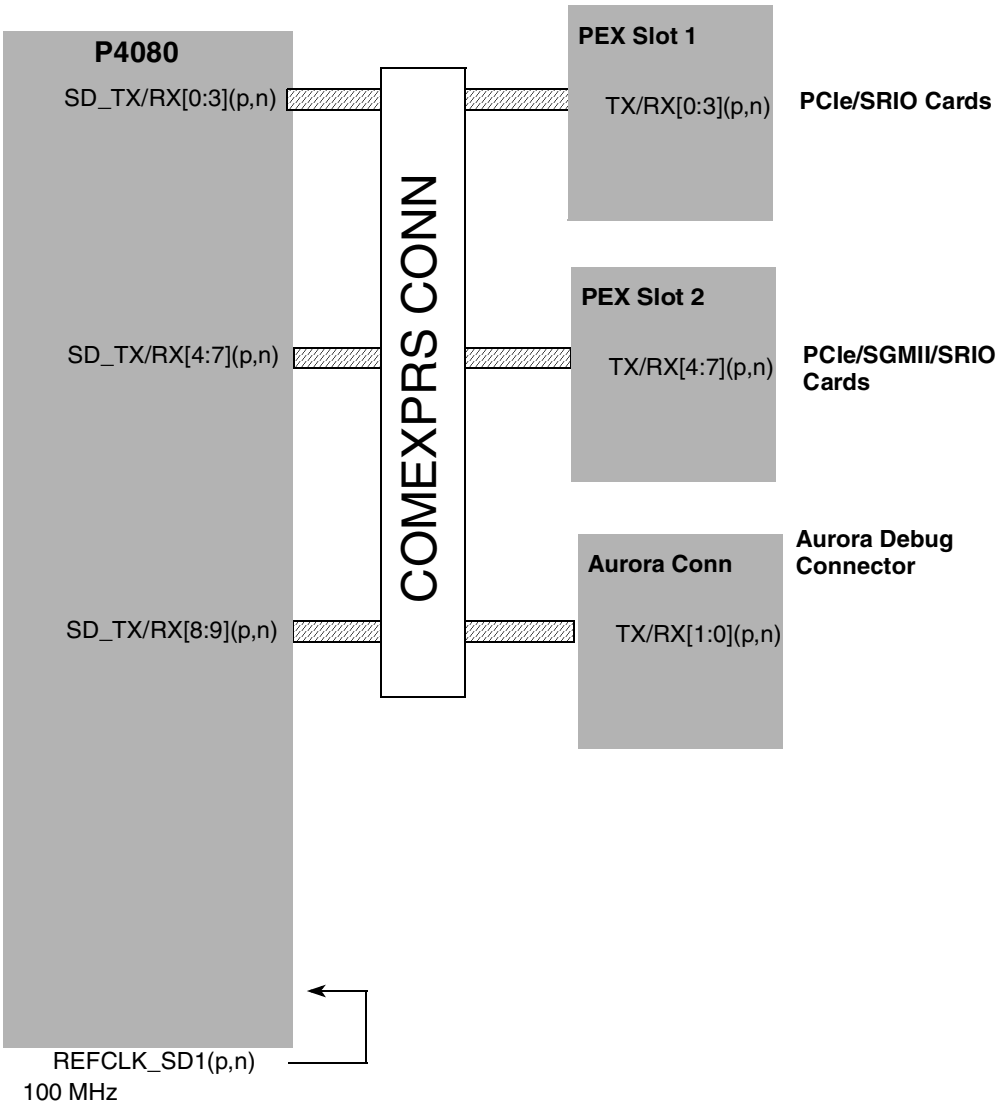


Figure 9. P4080 SerDes Bank1 to Carrier Board Cards/Debug Connector Configuration

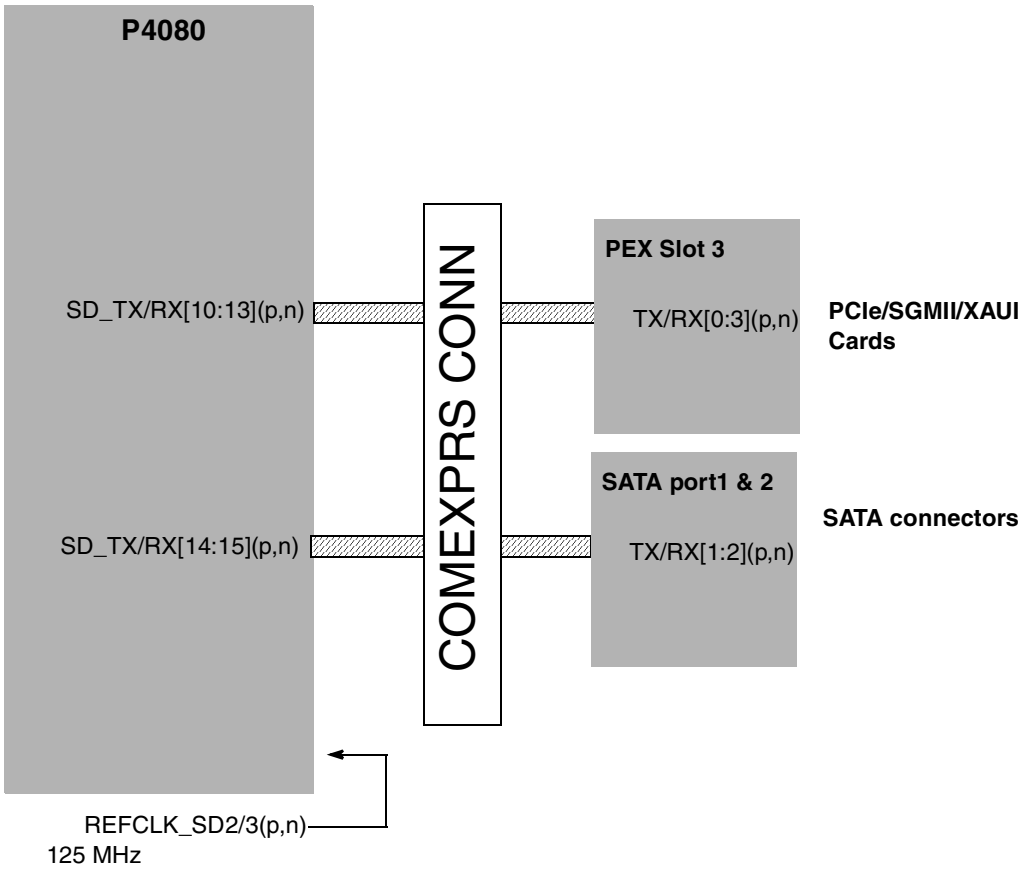


Figure 10. P4080 SerDes Bank 2 and 3 to Carrier Board Cards/SATA Connector Configuration

NOTE

The SD2 and SD3 clocking domains use separate clock generators.

2.3.3 Carrier Board Use of P4080 Ethernet Controller (EC) Interfaces

The carrier board uses up to two 10/100/1000baseT triple-speed Ethernet controllers (ECs) of the P4080 in one of the following configurations:

- EC2 is connected to the on-board PHY using the RGMII protocol; the remaining ports are unused.

  or
- Both ECs are independently connected to a ULPI USB interface; for the COMExprsDS, EC2 routes via the ULPI to a USB PHY.

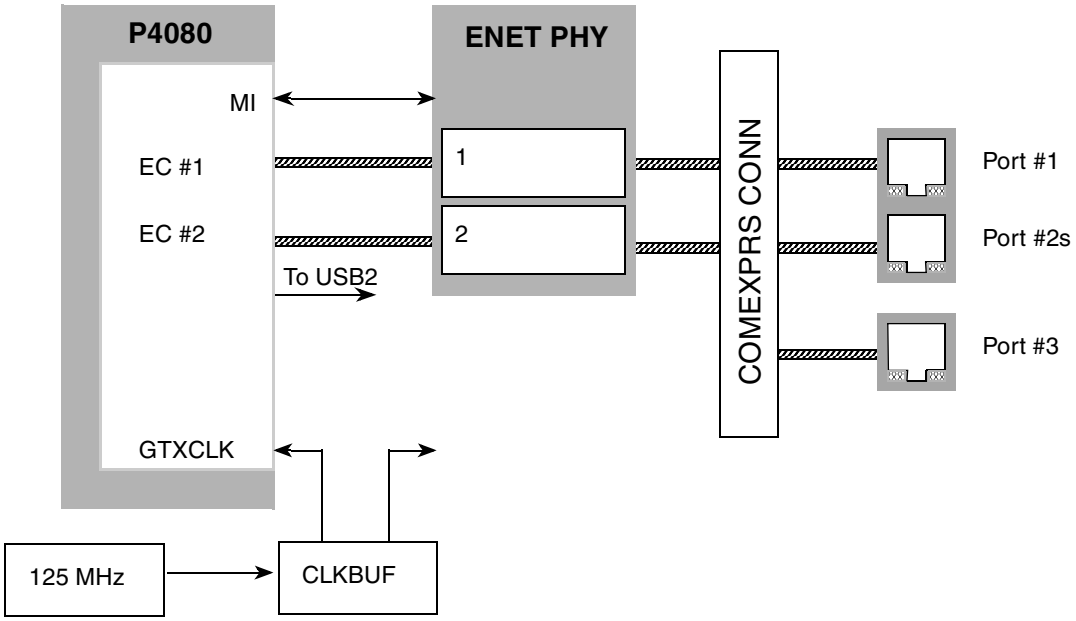


Figure 11. P4080 Ethernet Connections to the Carrier Board

Table 7 summarizes the carrier board EC connections and routing when the COMe1 is populated with a P4080.

Table 7. P4080 Ethernet Port Locations on Carrier

P4080 EC #	Connection Port	PHY Address	Location
1	1	0	Conn. P9 top
2	2	1	Conn. P9 bottom

See Section 2.3.8, "Carrier Board Use of P4080 USB Interfaces," and *COMX-P4080 COM Express Module* installation and user manual for more details on the use of these interfaces.

2.3.4 Carrier Board Use of P4080 Support for IEEE Std 1588™ Protocol

The carrier board supports the P4080 IEEE 1588 precision time protocol (PTP) as shown in Figure 12. This facility works in tandem with an Ethernet controller to time-stamp incoming packets.

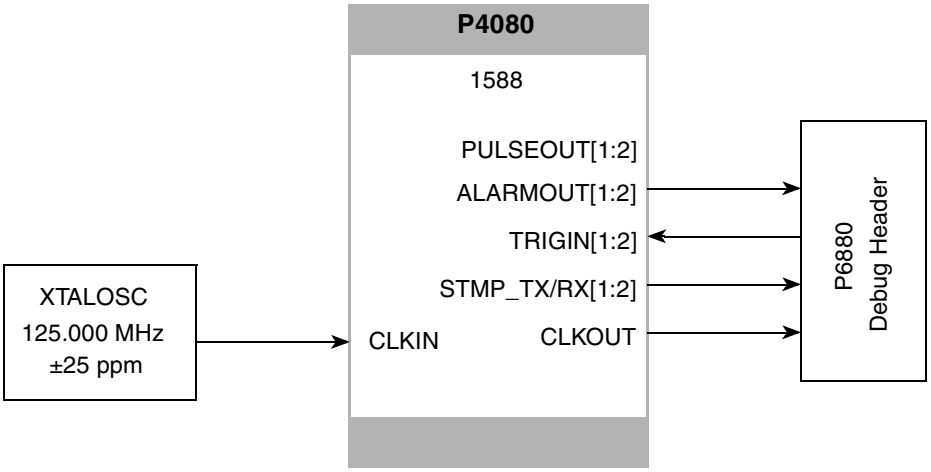


Figure 12. P4080 IEEE 1588 Interface to Carrier Board P6880 Debug Header

2.3.5 Carrier Board Use of P4080 Local Bus Interface

See the *COMX-P4080 COM Express Module* installation and user manual for details. Local bus connection to the carrier board is for Freescale internal use only.

2.3.6 Carrier Board Use of P4080 eSDHC Interface

The P4080 has an enhanced secure digital host controller (eSDHC). The carrier board connects the P4080 eSDHC to an SDMedia card slot and uses GPIO signals for sideband signals, such as write-protect-detect and card-detect. Both x4 and x8 cards are supported, the latter using the SPI_CS_B[0:3] signals, which can be reassigned as eSHDC_D[4:7].

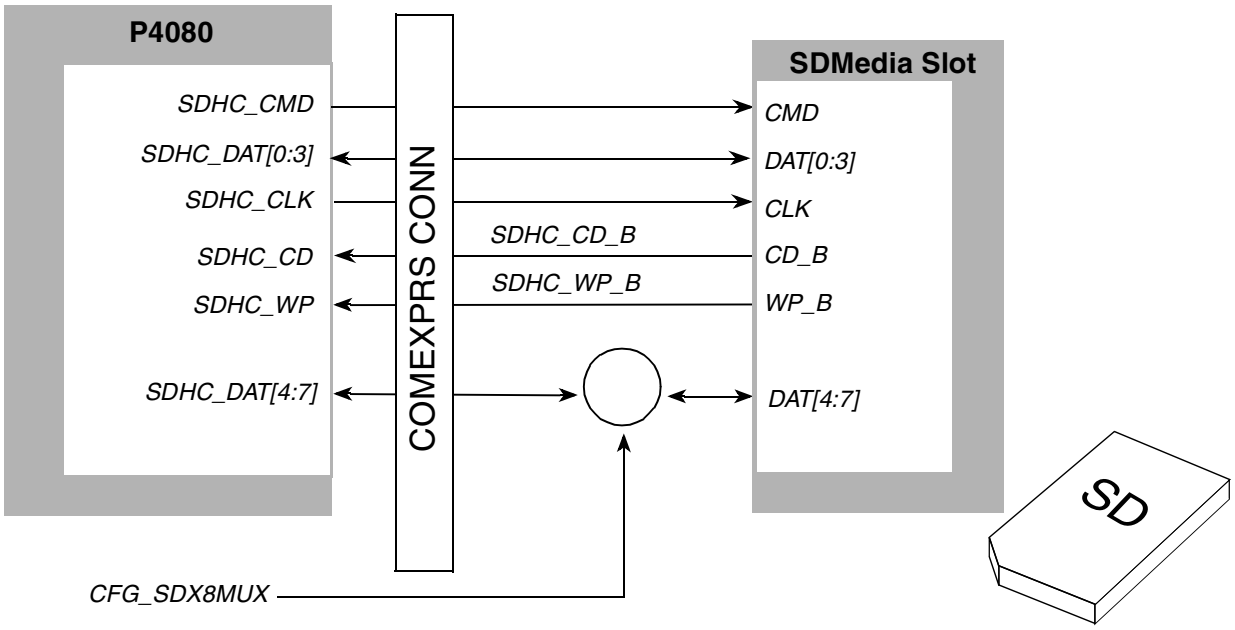


Figure 13. P4080 eSDHC Interface to Carrier Board SD Media Card Slot

NOTE

SDHC_DAT[4:7] are shared with the SPI CS pins; the CFG_SDX8MUX switch selects the routing of those pins to either the SDHC devices or the SPI devices, but both cannot be used simultaneously.

2.3.7 Carrier Board Use of P4080 SPI Interface

The P4080 has a serial peripheral interface (SPI), which is used to communicate with various peripherals. The COM Express carrier board connects a conventional 16-Mbyte serial SPI FLASH EEPROM to one chip-select of the P4080 SPI interface. The remaining three chip-selects are unused.

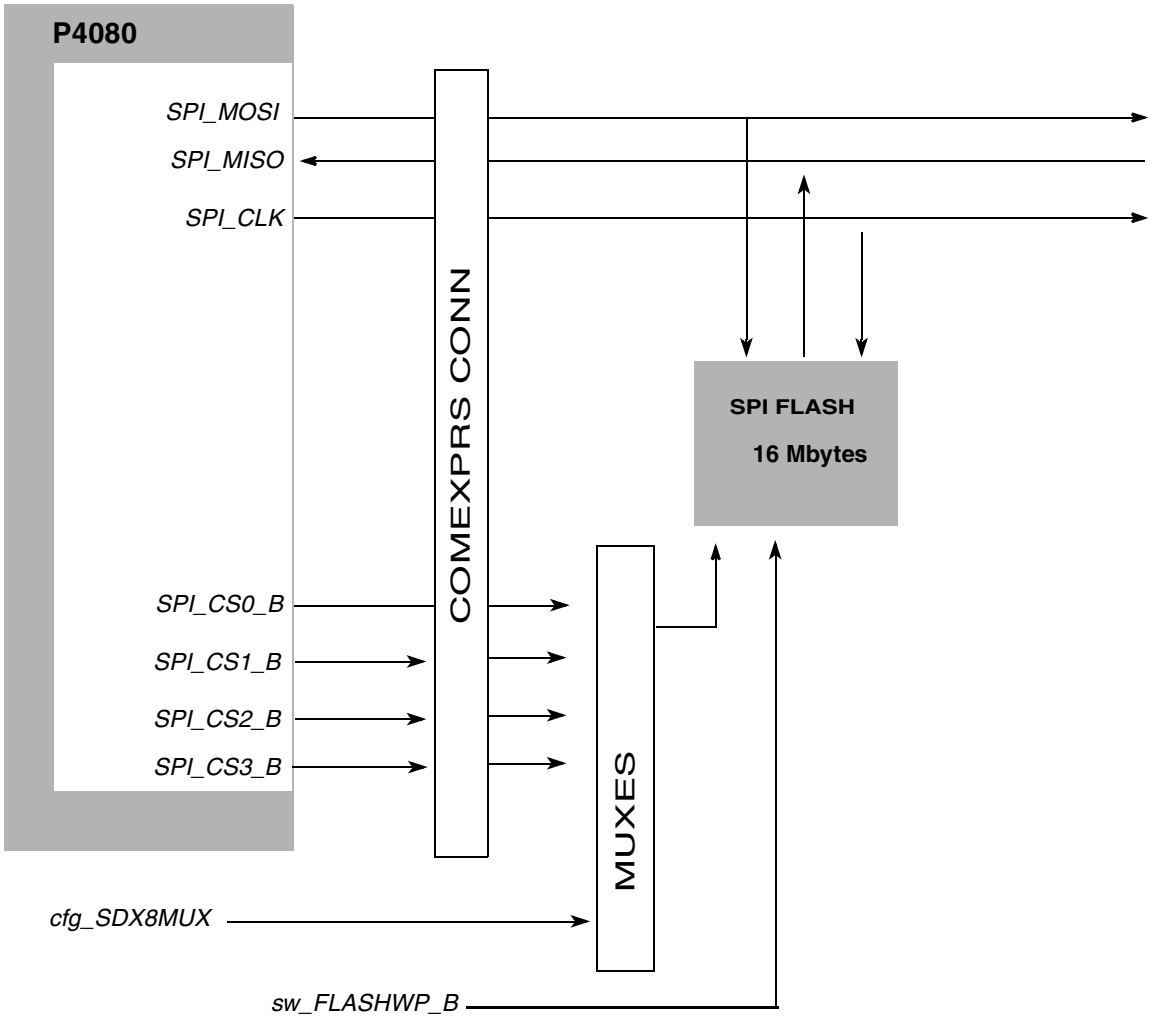


Figure 14. P4080 SPI Interface Connection to Carrier SPI FLASH Slot

2.3.8 Carrier Board Use of P4080 USB Interfaces

The P4080 has a USB 2.0 port that uses the UTMI+ protocol to connect to an external USB PHY, and it may be configured for host or device modes of operation.The carrier board USB port connector is a female "Type A" (the standard connector for a host to communicate with keyboards, mice, memory sticks, and so on).

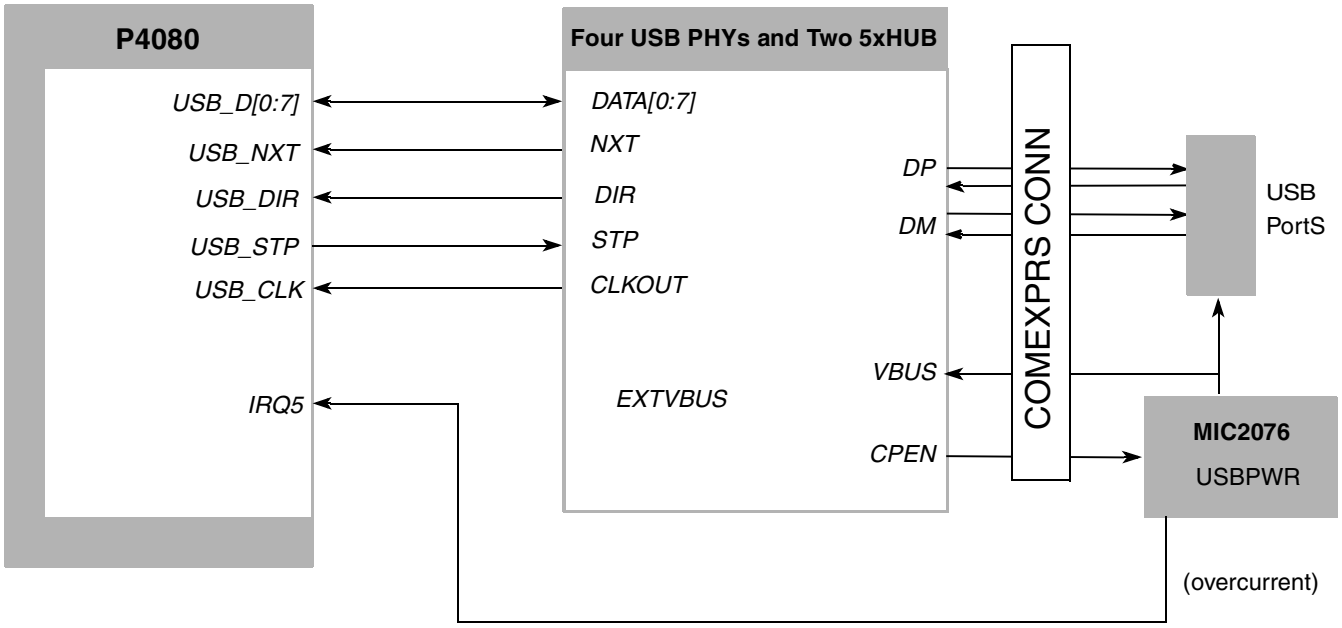


Figure 15. P4080 USB Connection to Carrier Board USB Interfaces

See the *COMX-P4080 COM Express Module* installation and user manual for details about the four PHYs and the two 5xHUBs.

2.3.9 Carrier Use of P4080 DMA Controllers

The P4080 DMA controllers have internal and external controls to initiate and monitor DMA activity. The carrier board does not incorporate any specific devices that make use of the external pin-controlled DMA controllers.

The P4080 DMA ports are connected to test points on the carrier board to allow external hardware control, as needed.

2.3.10 Carrier Use of P4080 eOpenPIC Interrupt Controller

The carrier board contains numerous interrupt connections. The P4080 eOpenPIC connections to the carrier are shown in Table 8. See the *COMX-P4080 COM Express Module* installation and user manual for more details on all of the interrupt signals implemented by the module.

Table 8. P4080 eOpenPIC Interrupt Connections to Carrier Board Devices

Signal Name	Connections
IRQ0_B	SLOT3 sideband connector (SGMII riser does not connect; must use in-band irq)
IRQ1_B	DS3232 real-time CLOCK and NVRAM
IRQ2_B	—
IRQ3_B	—
IRQ4_B	—
IRQ5_B	MIC2076 USB Power FLAG for over current at USB connector
IRQ6_B	—
IRQ7_B	Not connected
IRQ8_B	FPGA-TBD
IRQ9_B	FPGA-TBD
IRQ10_B	—
IRQ11_B	—
IRQ_OUT_B	Not used as Interrupt, but as an EVT pin

2.3.11 Carrier Use of P4080 GPIO Signals

The I^2C1 interface on the P4080 is expanded by routing five P4080 GPIO signals to the carrier board FPGA for general usage and routing three GPIO signals for controlling the IXXAT module. In the future, the FPGA could alternatively be implemented to use these GPIO signals to support EMI MDIO bus multiplexing as shown in Table 9. Currently, switches can be used, or the FPGA can automatically detect that I/O cards are in slots 2 and 3 and set the EMI value accordingly.

Table 9. Future Options for Configuring P4080 Dedicated GPIO Signals for EMI MDIO Bus Multiplexing

Signal Name	System Function
GPIO[0:1]	EM1 management bus mux control
GPIO[2:3]	EM2 management bus mux control
GPIO[4:7]	Spares connected to test points

2.3.12 Carrier Use of P4080 Control Signals

The carrier board implements SYS_RESET_B to reset the entire development system, and CB_RESET_B in turn sends a reset to the FPGA from the COMe module.

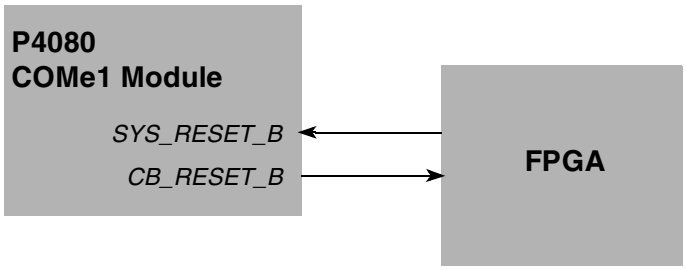


Figure 16. P4080/COMe1 System Reset Connection with Carrier Board FPGA

2.3.13 Carrier Board Use of P4080 UART Serial Ports

The carrier board connects both 4-wire serial ports of the P4080 to serial level transceivers, and from there to a stacked dual DB9 male connector placed on the front panel UART I/O board that is located at the front of the chassis. The default mode is 4-wire, so RTS/CTS flow control is supported on these connectors. For the P4080DS kit (P4080COMe-DS-PB), UART ports 0 and 1 are supported.

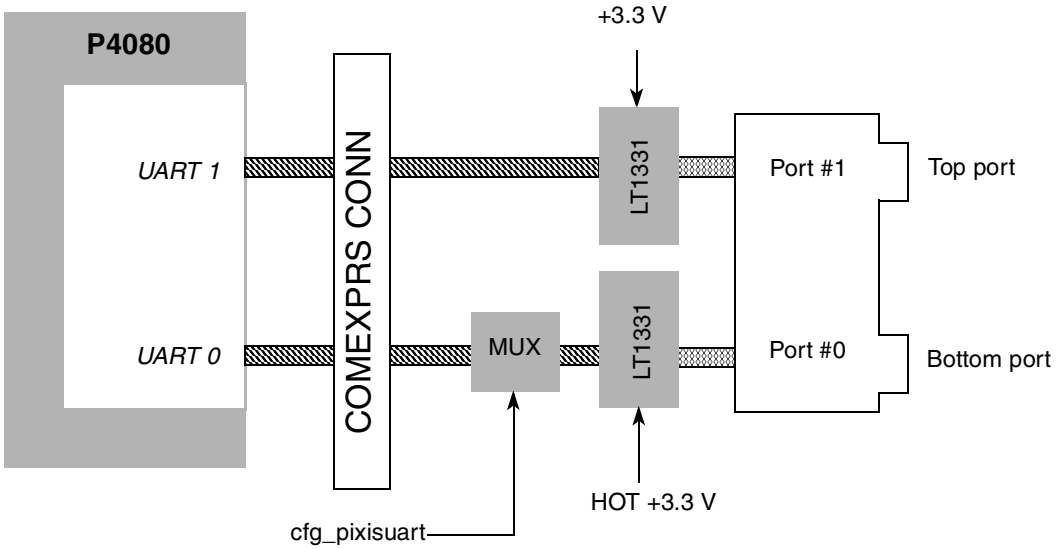


Figure 17. P4080 UART Serial Port Connection to Carrier Board Serial Port Connector

2.3.14 Carrier Board Use of P4080 I²C Interfaces

The carrier board uses three of the four available I²C/SMB buses. The I²C1 master from the FPGA accesses the EEPROM on the COMe module to read 256 bytes of EEPROM (processor type) data before the carrier system reset is asserted to the module

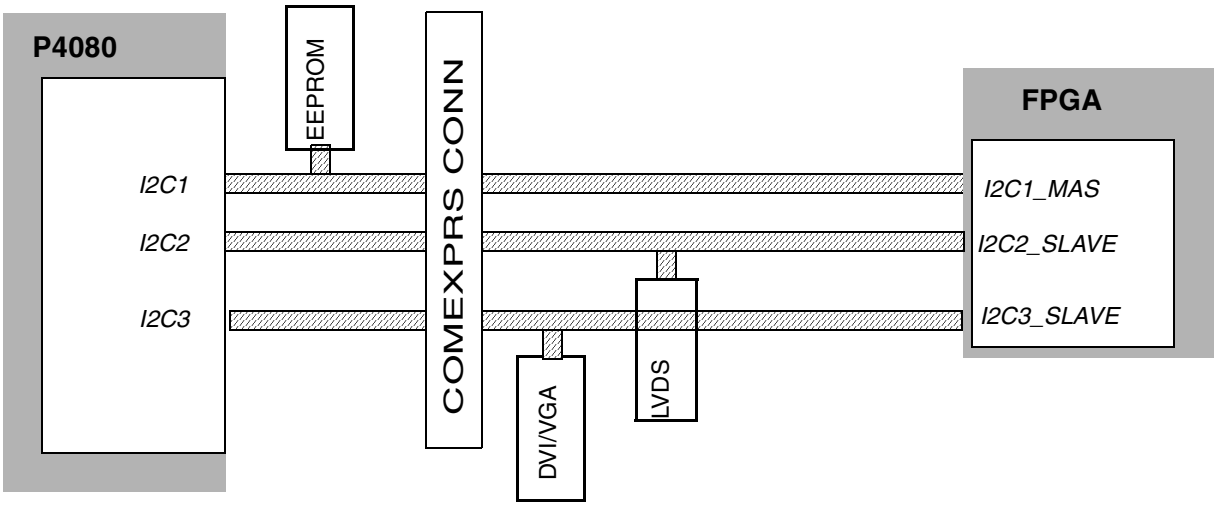


Figure 18. IP4080 I²C Connectivity to Carrier Board FPGA

The P4080 I²C bus device addresses on the carrier board are summarized in Table 10.

Table 10. P4080 I²C Bus Device Map for Carrier Board

I²C Bus	I²CAddress	Device	Notes
1	0x21	Reserved	—
1	0x22	Reserved	—
1	0x23	IO Expander Philips PCA9555PW	Not used for P4080 module. Reserved.
1	0x34	CODEC Wolfson WM8776SEFT	Not used for P4080 module. Reserved.
1	0x64	DDR3 DIMM2	On P4080 COMe module
1	0x66	DDR3 DIMM1	On P4080 COMe module
1	0x98	Thermal sensor ON Semiconductor ADT7461ARMZ	On P4080 COMe module
1	0xA0	4-Kbyte EEPROM Atmel AT24C02C or equivalent	Boot configuration I²C EEPROM on P4080 COMe module
1	0xA4	Remote I²C IO Expander Philips PCA9672PW Device ID	On carrier. Read only. See datasheet for programming instructions
1	0xA8	4-Kbyte EEPROM Atmel AT24C64A or equivalent.	Stores 256 bytes of processor type data. Write protectable.
1	0xD0	RTC	On P4080 COMe module

Table 10. P4080 I²C Bus Device Map for Carrier Board (continued)

I²C Bus	I²CAddress	Device	Notes
1	0xDC	Clockgen for SD BANK1 IDT 9FG104DGILFT	On P4080 COMe module
1	0x57	I²C slave port	Not used for P4080. Reserved.
2	0x58	USB HUB2	On P4080 COMe module
2	0x60	6-bit DAC Maxim MAX5362LEUK	Not used for P4080 module. Reserved.

Note: These addresses do not include the position of the LSB of the transmitted address (the read/write bit).

See Section 4, "Programming Model," for I²C implementation information.

2.3.15 Carrier Board Use of P4080 EM1 and EM2 Management Buses

The P4080 has the following types of buses:

- SGMII and RGMII PHY management
- XAUI PHY management

Because one set of buses must span across multiple devices on the carrier board, multiplexers are used to route from the P4080 to each PHY, and switches are used to control these multiplexers.

PHY management bus control is summarized in Table 11 and Table 12.

Table 11. P4080 PHY Management Bus Map for EMI1 on Carrier Board

Bus	SW4[3:4]	Device
EMI1	00	On board RGMI PHYI
EMI1	01	Slot 2 SGMII
EMI1	10	Slot 3 SGMII

Table 12. P4080 PHY Management Bus Map for EMI2 on Carrier Board

Bus	SW8[4:5]	Device
EMI2	00	No Device
EMI2	01	No Device
EMI2	10	No Device
EMI2	11	Slot 3 XAUI

2.3.16 Carrier Board Use of P4080 Debug Features

The carrier board provides a JTAG COP header and AURORA test points for debug purpose using the CodeWarrior USBTAP already installed in the system.

To upgrade the U-Boot stored on the COMe module's NOR FLASH, use the CodeWarrior USBTAP tool. See the *COMX-P4080 COM Express Module* installation and user manual and *Mentor Embedded Linux For Freescale COMe P2020 System Builder Quick Start Guide* for more details.

2.3.17 Carrier Board Clock Generation from P4080 COMe1 Module Board

The carrier board clock signals are generated by the COMe module board in use. Table 13 lists the requirements of the carrier board clock signals when the carrier board is populated with a P4080 COMe1 module. For more details on the P4080 COMe1 module, see the *COMX-P4080 COM Express Module* installation and user manual.

Table 13. Carrier Board Clock Requirements When Used with P4080 COMe1 Module

COMe1 Clock Signal	Corresponding Carrier Board Clock Signal	Clock Frequency	Type
SD1 REFCLK	SLOT1 REFCLK(p,n)	—	LVDS
SD2 REFCLK	P4080 SD2_REFCLK(p,n) SLOT2 REFCLK(p,n) SLOT3 REFCLK(p,n)	156.25 MHz or 125.00 MHz	LVDS
SD3 REFCLK	P4080 SD3_REFCLK(p,n)	156.25 MHz or 125.00 MHz	LVDS
	SLOT5 REFCLK(p,n)	—	LVDS

Figure 19 shows the principal clock connections from the P4080 COMe1 module to the carrier board.

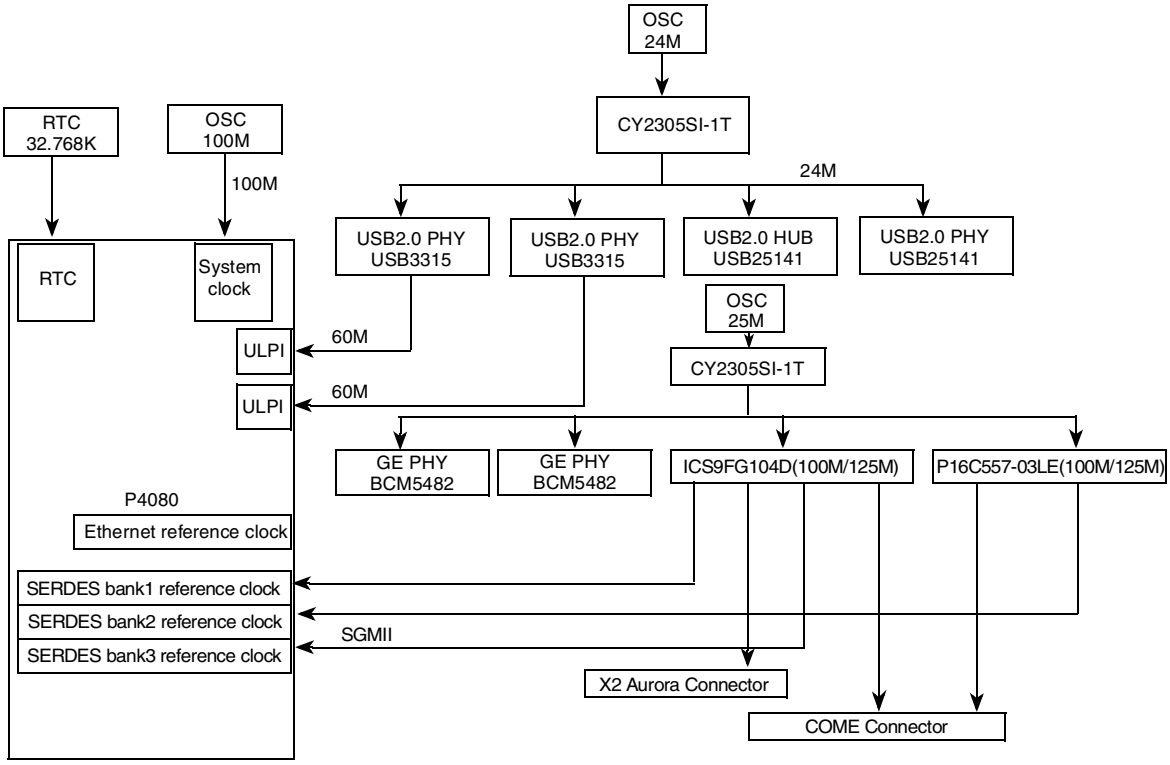


Figure 19. P4080 COMe1 Module Clock Architecture

Conversely, the carrier board provides a battery to the RTC clock to keep time while the system is turned off as shown in Table 14.

Table 14. P4080 Clock Connections to Carrier Board

Pin Count	Signal Names	Connections
1	RTC	Arbitrary timebase frequency
11	Total pins in this group	

NOTE

The SerDes and Ethernet clocks are described in their respective sections.

2.3.18 P4080 Power

An ATX power supply (600 W) is provided in the system to support the P4080 COMe1 module, the carrier board and all its I/O cards. VCC_12, VCC_5V_STBY, and VCC_RTC_BAT are provided to the COMe module from the carrier board.

3 COM Express Carrier Architecture When Used with COMe2-Type Module

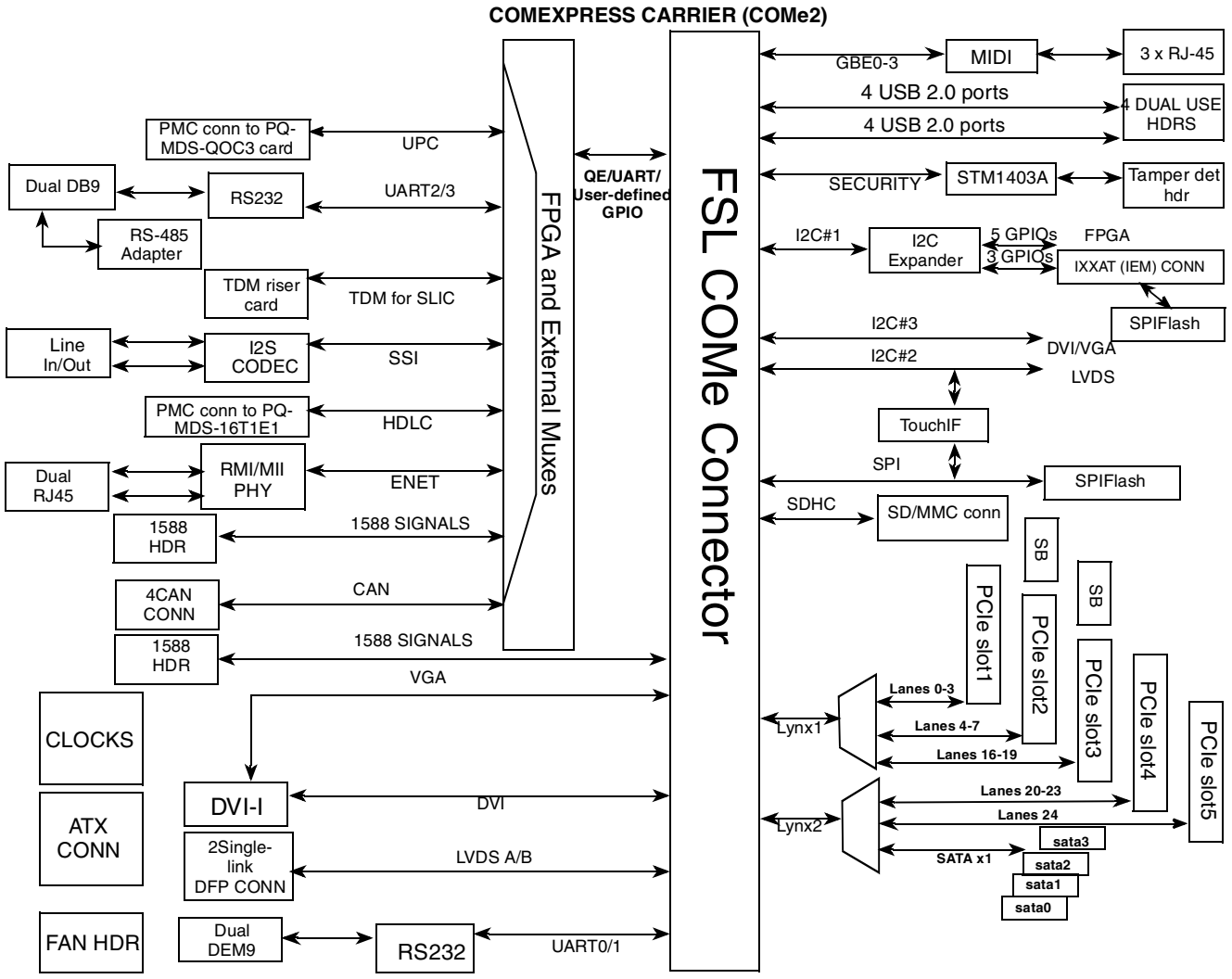


Figure 20. COM Express Carrier Block Diagram When Used with COMe2-Type Module

3.1 System Reset Performed by FPGA Reset Sequencer in a System with a COMe2 Module

The carrier board FPGA contains a reset sequencer that properly manages the orderly bring-up of the system (this is not the same as the power sequencer, which is similar, but not specifically related to reset).

After the system transitions to having fully stable power supplies, the reset sequencer does the following:

1. Waits for all reset conditions to clear
2. Configures and releases the processor from reset
3. Idles waiting for further reset conditions to occur

Table 15 summarizes the reset conditions and actions of the FPGA when used with a COMe2 module.

Table 15. Reset Conditions and Actions of FPGA Reset Sequencer

Term	Type	Description	Notes
HOT_RST_B	External	HOT power stable	Restarts all CPLD power sequencing
PWRGD	External	ATX power stable	Causes full system reset unless the system is in S3 (power down) state.
SYS_RST_B	External	COP tool reset request	Upon power good, sys_rst_b is sent from carrier to COMe2 module.
RESET_REQ_B	External	CPU requests reset	Full reset

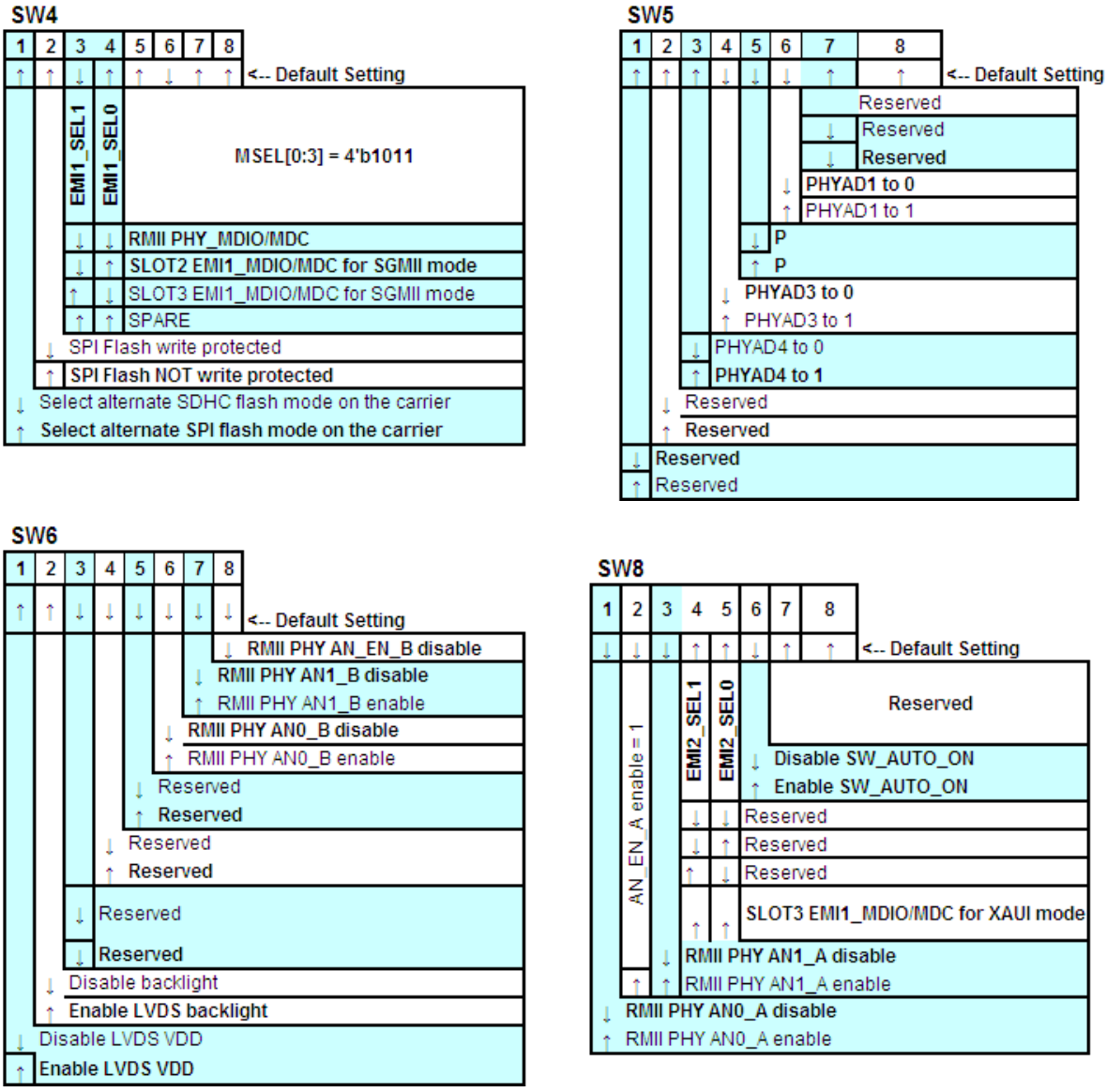
3.2 Carrier Board Configuration Switches in a System with a P2020 COMe2 Module

There are different types of COMe configurations. A list of these configuration types and their implementation is shown in Table 16.

Table 16. Carrier Board Configuration Types

Configuration Type	Implementation
Requires software configuration to support evaluation	Implemented with “DIP switches” and/or software-settable options
Expected to be easily and often changed by the end-user or developer	

The carrier board switches and their default settings when used with a P2020 COMe module are shown in Figure 21. Switch names exactly match the name on the schematics and on the printed-circuit board in most cases, except where a spare has been newly assigned and only the FPGA has changed.



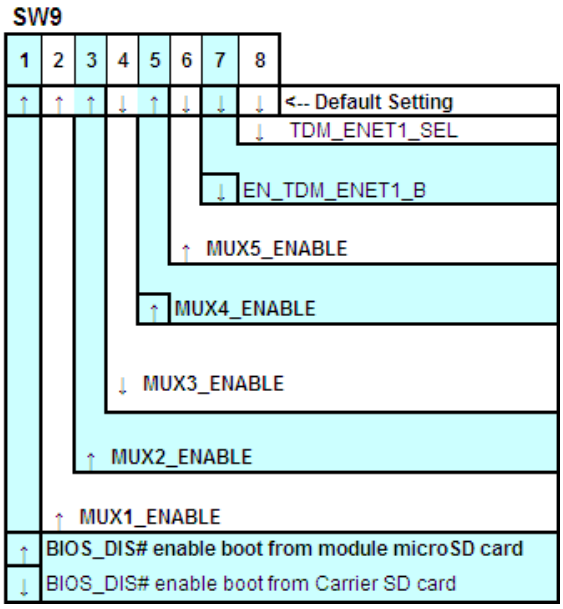


Figure 21. Carrier Board Switch Assignments and Defaults When Used with P2020 COMe Module

For those signals configured using switches, the configuration logic is as shown in Figure 22.

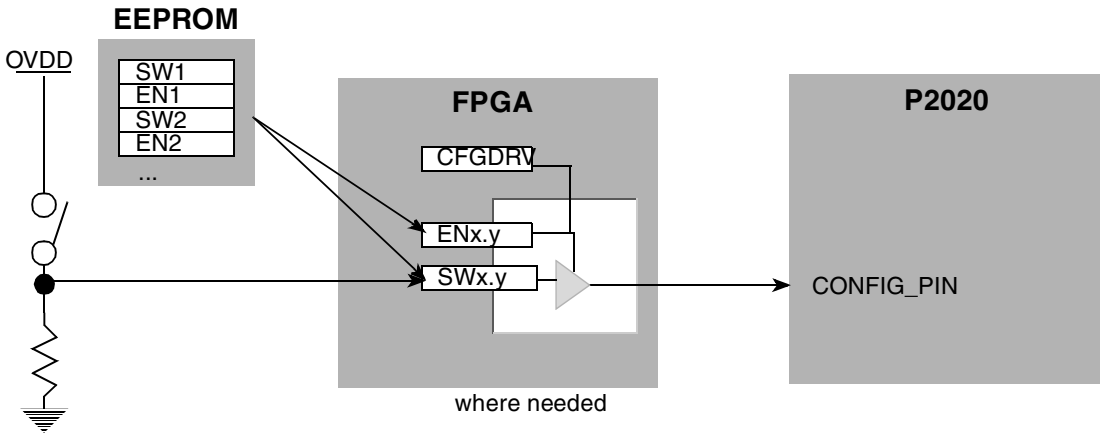


Figure 22. COMe2 Configuration Switch Logic and P2020

The default action is for the FPGA to transfer the switch setting to the processor configuration pin during the CB_RESET_B assertion interval.

For certain COMe modules, the I^2C expander FPGA IO signals can select the multiplexer configurations.

3.3 COM Express Carrier Board Functionality when Used with a P2020 COMe2 Module

This section and its subsections are tailored to the carrier board functionality when used with the P2020 COMe2 module specifically.

Figure 23 shows the P2020 COMe module block diagram. Note that functional modules that only exist on the COMe module are described in the *COMX-P4080 COM Express Module* installation and user manual.

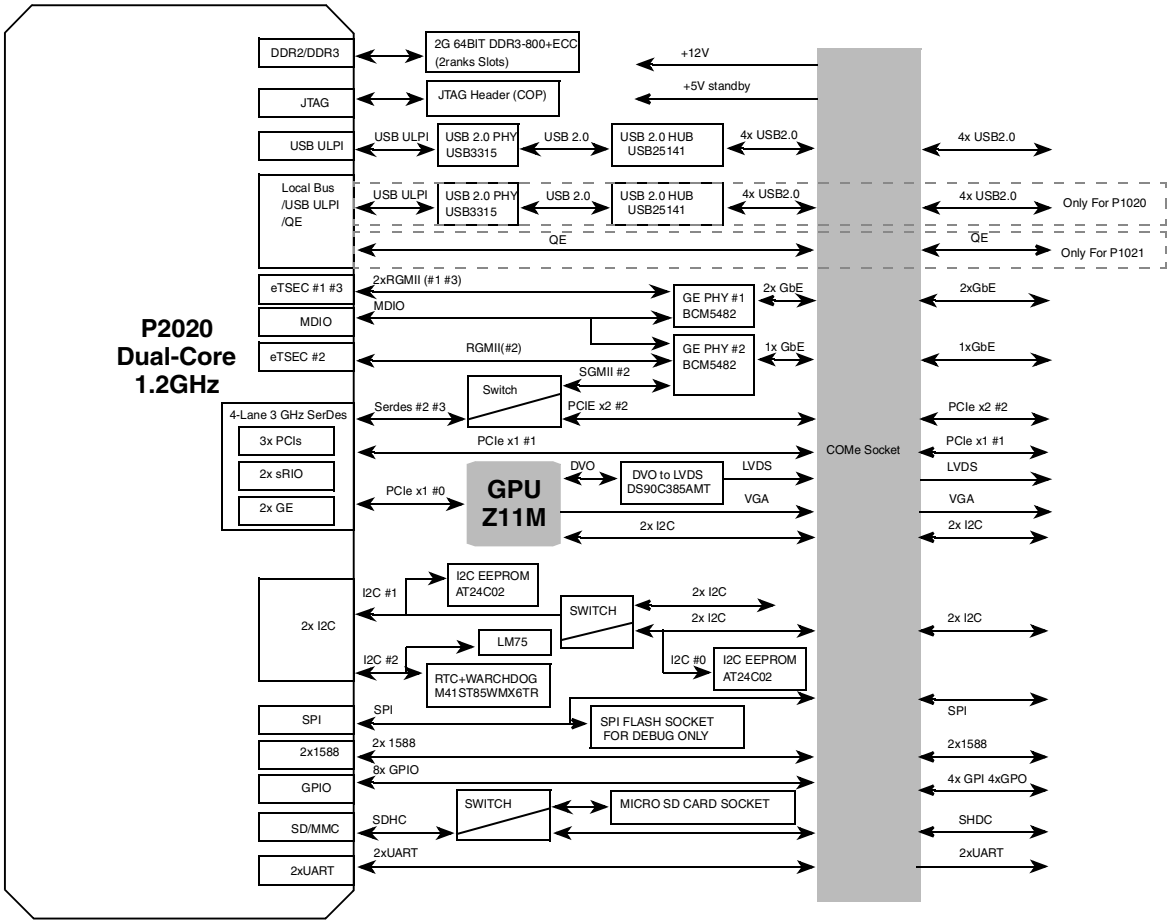


Figure 23. P2020 COMe Module Block Diagram

3.3.1 Carrier Board Use of P2020 DDR Interface

See the *COMX-P2020COM Express Module* installation and user manual.

3.3.2 Carrier Board Use of P2020 SerDes x18 Interface

The SerDes block on the P2020 provides high-speed serial communications interfaces for several internal devices. The SerDes block on the P2020 COMe2 provides 18 serial lanes for the carrier that may be partitioned as shown in Table 17.

Note that the term ‘lane’ is used to describe the minimum number of signals needed to create a bidirectional communications channel; in the case of PCI-Express or Serial RapidIO, a lane consists of two differential pairs, one for receive and one for transmit, or four in all.

Table 17, top down, shows the following clocking banks and how they are configured by the carrier board:

- Bank1—lanes 0–3 go to slot 1
- Bank2—lanes 4–7 go to slot 2
- Bank3—lanes 16–17 go to slot 3

Table 17. P2020 SerDes Lane Multiplexing Configurations on Carrier

Bank 1				Bank 2				Bank 3	
A	B	C	D	E	F	G	H	C	J
0	1	2	3	4	5	6	7	16	17
SLOT 1	—			SLOT 2	—			SLOT 3	
PCIe1 (5/2.5G)	—			PCIe2 (5/2.5G)	—			PCIe3 (5/2.5G)	

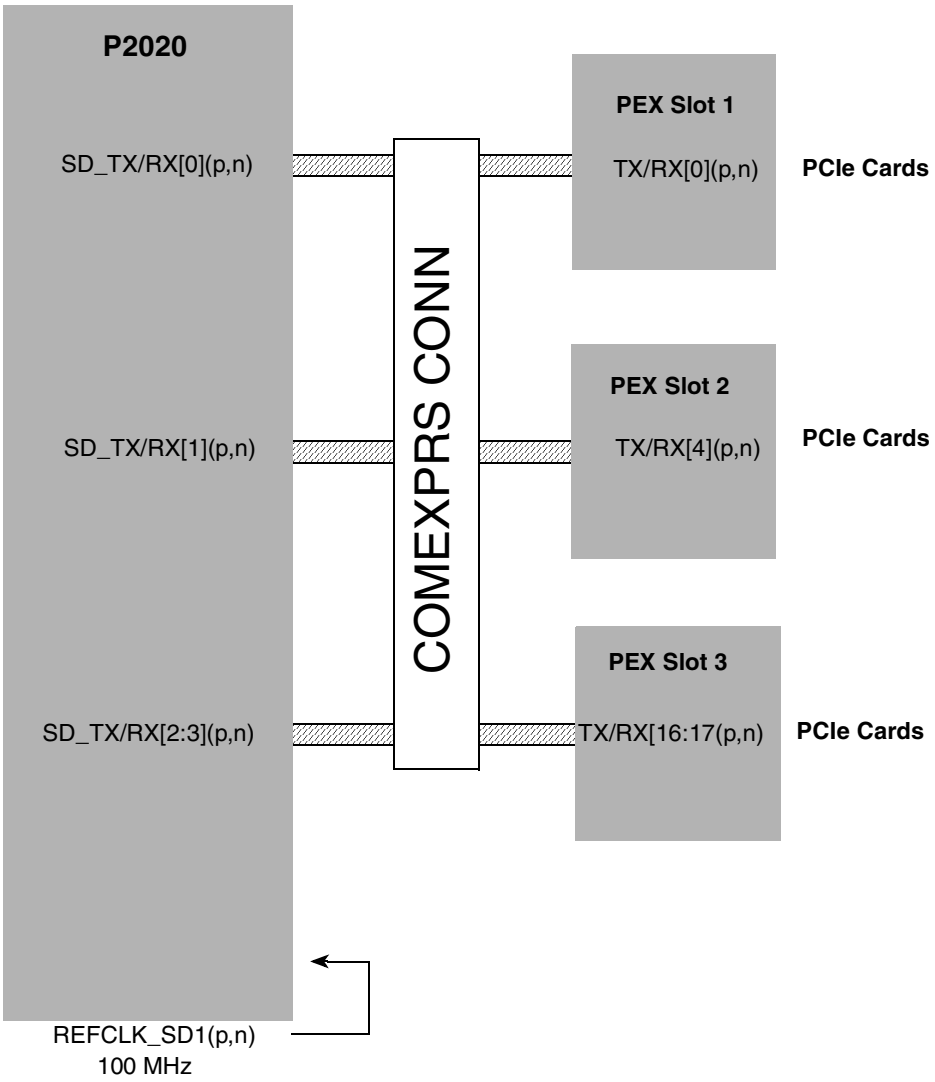


Figure 24. P2020 SerDes Bank1 to Carrier Board Cards Configuration

NOTE

The SD2 and SD3 clocking domains use separate clock generators.

3.3.3 Carrier Board Use of P2020 Ethernet Controller (EC) Interfaces

The carrier board uses up to two 10/100/1000baseT triple-speed Ethernet controllers (ECs) of the P2020 as follows:

- EC2 is connected to the on-board PHY using the RGMII protocol; the remaining ports are unused.

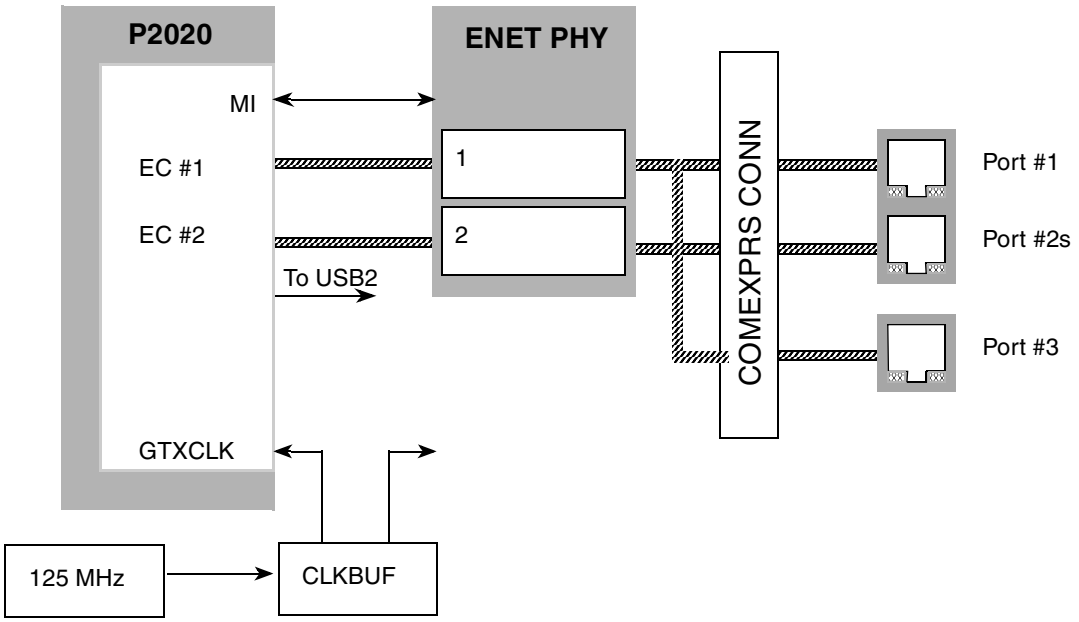


Figure 25. P2020 Ethernet Connections to the Carrier Board

Table 18 summarizes the carrier board EC connections and routing when the COMe2 is populated with a P2020.

Table 18. P2020 Ethernet Port Locations on Carrier

P2020 EC #	Connection Port	PHY Address	Location
1	1,3	0,1	P9 top, P11
2	2	2	P9 bottom

See Section 3.3.8, “Carrier Board Use of P2020 USB Interfaces,” and the *COMX-P2020 COM Express Module* installation and user manual for more details on the use of these interfaces.

3.3.4 Carrier Board Use of P2020 Support for IEEE Std 1588™ Protocol

The carrier board supports the P2020 IEEE 1588 precision time protocol (PTP) as shown in Figure 26. This facility works in tandem with the Ethernet controller to time-stamp incoming packets.

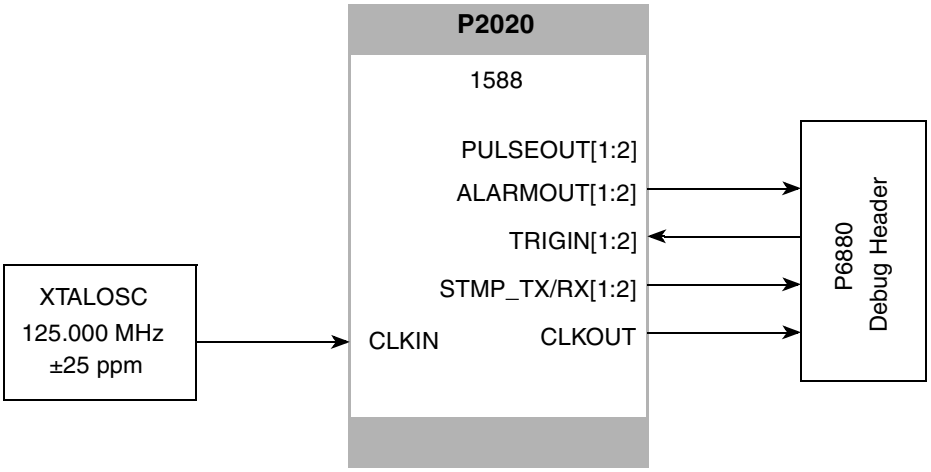


Figure 26. P2020 IEEE 1588 Interface to Carrier Board P6880 Header

3.3.5 Carrier Board Use of P2020 Local Bus Interface

See the *COMX-P2020 COM Express Module* installation and user manual for details on how the P2020 local bus interface is used.

3.3.6 Carrier Board Use of P2020 eSDHC Interface

The P2020 has an enhanced secure digital host controller (eSDHC). The carrier board connects the P2020 eSDHC to an SDMedia card slot and uses GPIO signals for sideband signals, such as write-protect-detect and card-detect. Both x4 and x8 cards are supported, the latter using the SPI_CS_B[0:3] signals, which can be reassigned as eSHDC_D[4:7].

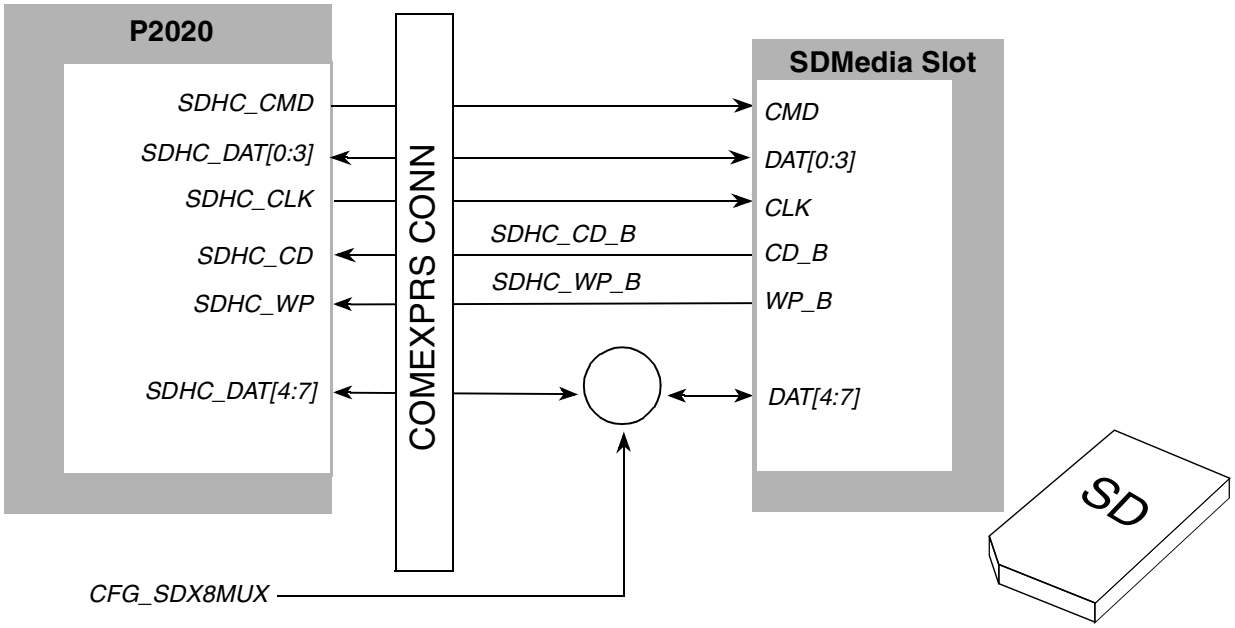


Figure 27. P2020 eSDHC Interface to Carrier Board SD Media Card Slot

NOTE

SDHC_DAT[4:7] are shared with the SPI CS pins; the CFG_SDX8MUX switch selects the routing of those pins to either the SDHC devices or the SPI devices, but both cannot be used simultaneously.

3.3.7 Carrier Board Use of P2020 SPI Interface

The serial peripheral interface (SPI) on the P2020 communicates with various peripherals. The COM Express carrier board connects a conventional, 16-Mbyte serial SPI FLASH EEPROM to one chip-select of the P2020 SPI interface. The remaining three chip-selects are unused.

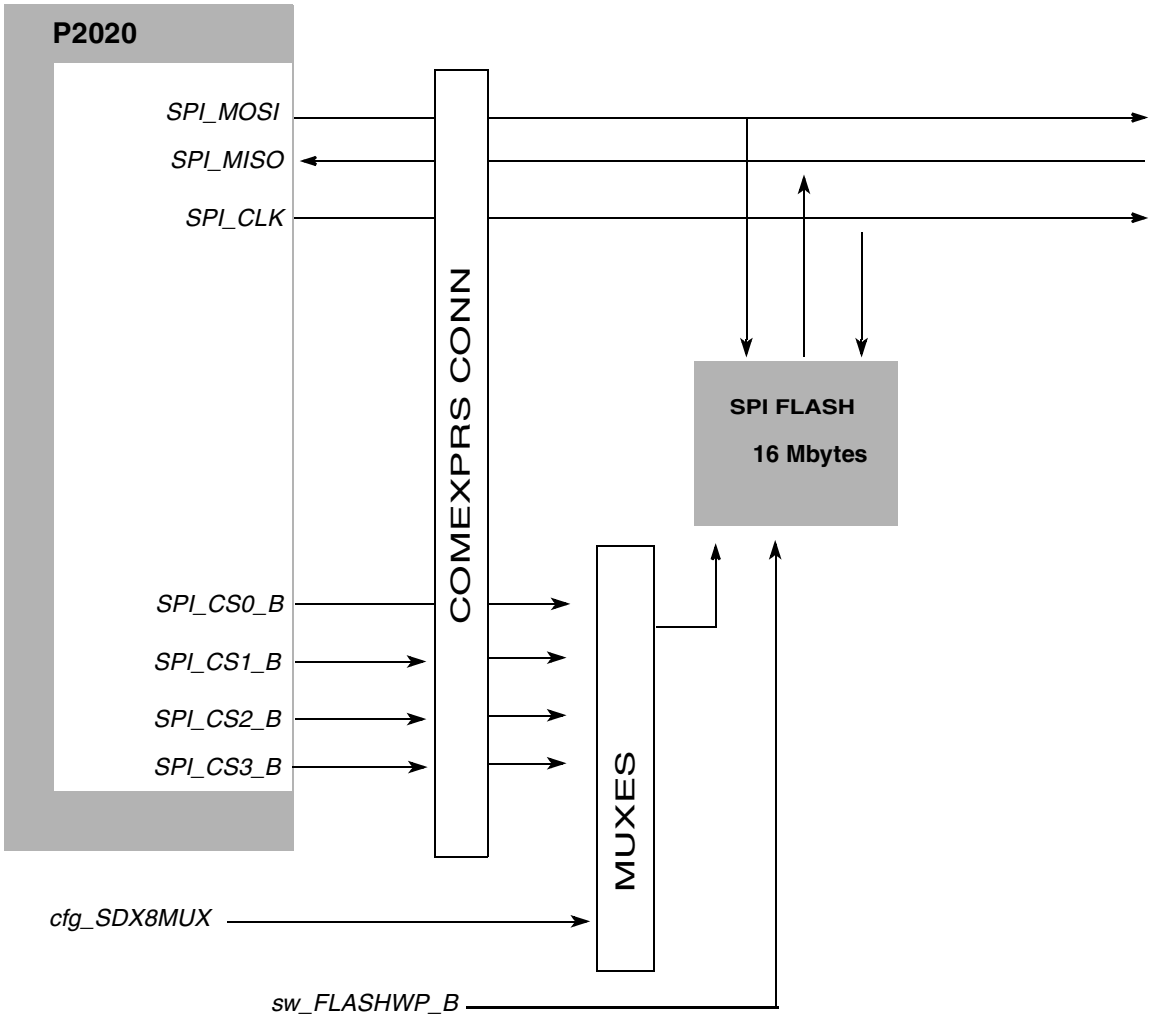


Figure 28. P2020 SPI Interface Connection to Carrier SPI FLASH Slot

3.3.8 Carrier Board Use of P2020 USB Interfaces

The P2020 has a USB 2.0 port that uses the UTMI+ protocol to connect to an external USB PHY, and it may be configured for host or device modes of operation. The carrier board USB port connector is a female "Type A" (the standard connector for a host to communicate with keyboards, mice, memory sticks, and so on).

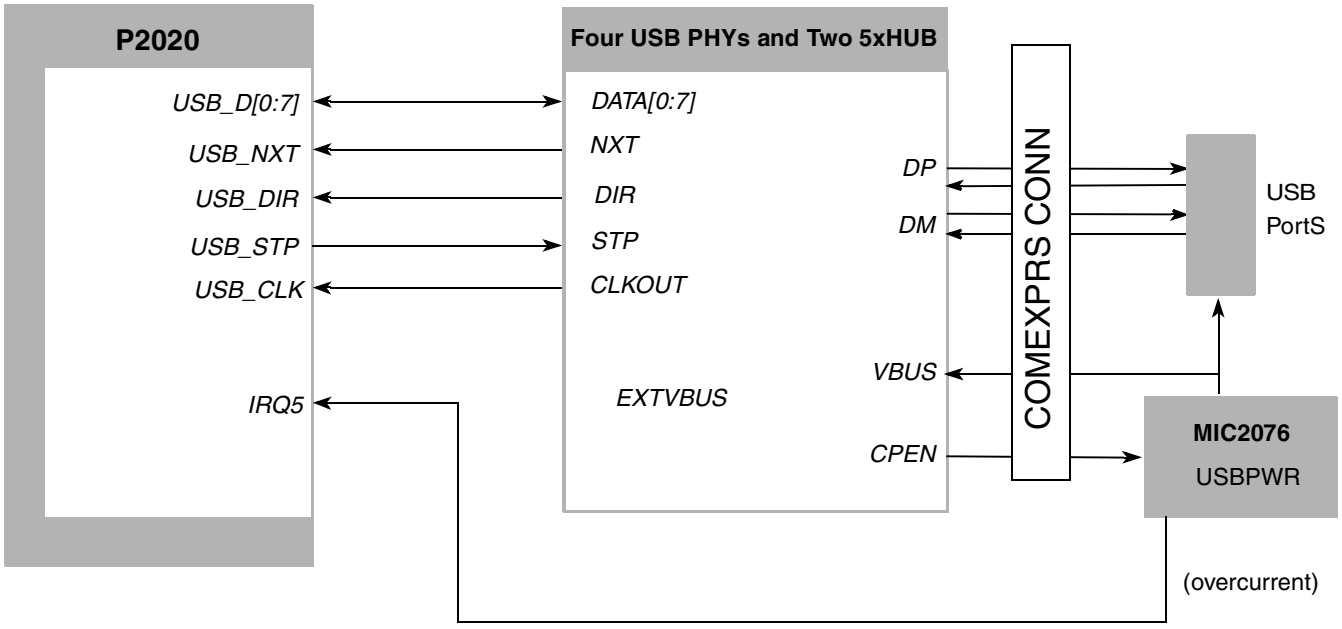


Figure 29. P2020 USB Connection to Carrier Board USB Interfaces

See the *COMX-P2020 COM Express Module* installation and user manual for details about the four PHYs and the two 5xHUBs.

3.3.9 Carrier Use of the P2020 DMA Controller

The P2020 DMA controllers have internal and external controls to initiate and monitor DMA activity. The carrier board does not incorporate any specific devices that make use of the external pin-controlled DMA controllers.

The P2020 DMA ports are connected to test points on the carrier board to allow external hardware control, as needed.

3.3.10 Carrier Use of P2020 eOpenPIC Interrupt Controller

The carrier board contains numerous interrupt connections. The P2020 eOpenPIC connections are as shown in Table 19. See the *COMX-P2020 COM Express Module* more details on all of the interrupt signals implemented by the module.

Table 19. P2020 eOpenPIC Interrupt Connections to Carrier Board Devices

Signal Names	Connections
IRQ0_B	SLOT3 Sideband connector (SGMII riser does not connect, must use in-band irq)
IRQ1_B	DS3232 real-time CLOCK and NVRAM
IRQ2_B	—
IRQ3_B	—
IRQ4_B	—
IRQ5_B	MIC2076 USB Power FLAG for over current at USB connector
IRQ6_B	—
IRQ7_B	Not Connected
IRQ8_B	FPGA—TBD
IRQ9_B	FPGA—TBD
IRQ10_B	—
IRQ11_B	—
IRQ_OUT_B	Not used as Interrupt, but as an EVT pin

3.3.11 Carrier Use of P2020 GPIO Signals

The I^2C1 interface on the P2020 is expanded by routing five P2020 GPIO signals to the carrier board FPGA for general usage and three GPIO signals for controlling the IXXAT module. In the future, the FPGA could alternatively be implemented to use these GPIO signals to support EMI MDIO bus multiplexing as shown in Table 20. Currently, switches can be used, or the FPGA can automatically detect that IO cards are in slots 2 and 3 and set the EMI value accordingly.

Table 20. Future Options for Configuring P2020 Dedicated GPIO Signals for EMI MDIO Bus Multiplexing

Signal Names	System Function
GPIO[0:1]	EM1 management bus mux control
GPIO[2:3]	EM2 management bus mux control
GPIO[4:7]	Spares connected to test points

3.3.12 Carrier Use of P2020 Control Signals

The carrier board implements SYS_RESET_B to reset the entire development system, and CB_RESET_B in turn sends a reset to the FPGA from the COMe module.

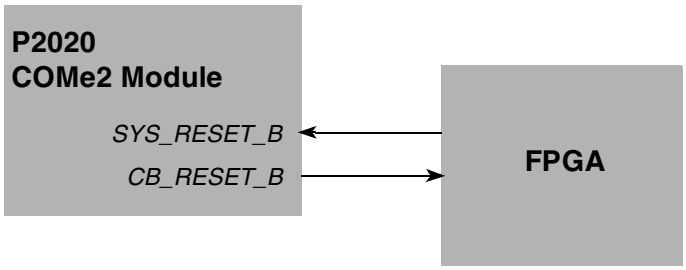


Figure 30. P2020/COMe2 System Reset Connection with Carrier Board FPGA

3.3.13 Carrier Board Use of P2020 UART Serial Ports

The carrier board connects both 4-wire serial ports of the P2020 to serial level transceivers, and from there to a stacked dual DB9 male connector placed on the front panel UART I/O board that is located at the front of the chassis. The default mode is 4-wire, so RTS/CTS flow control is supported on these connectors. For the P2020 DS kit (P2020COMe-DS-PB), UART ports 0 and 1 are supported.

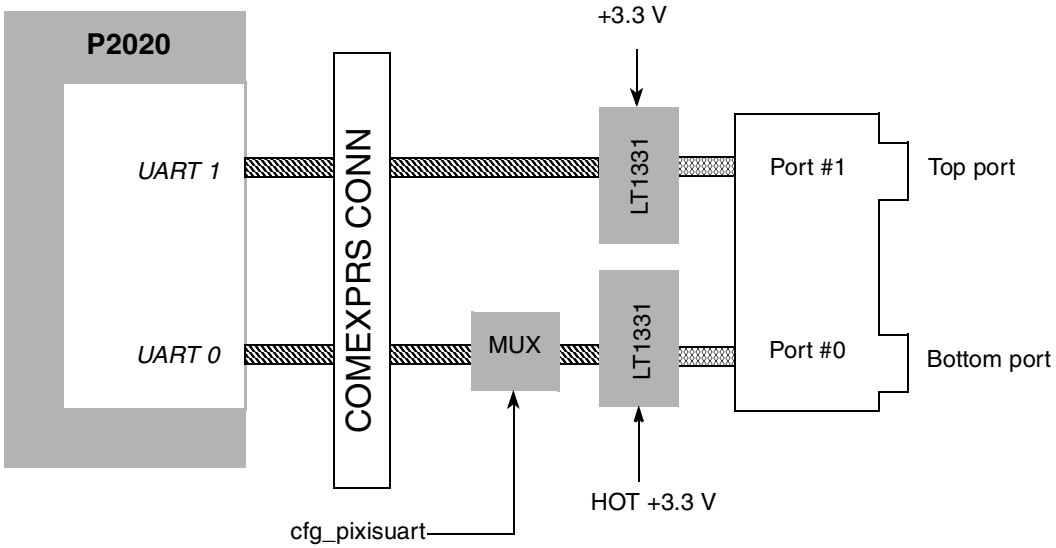


Figure 31. P2020 UART Serial Port Connection to Carrier Board Serial Port Connector

3.3.14 Carrier Board Use of P2020 I²C Interfaces

The carrier board uses three of the four available I²C/SMB buses. The I²C1 master from the FPGA accesses the EEPROM on the COMe module to read 256 bytes of EEPROM (processor type) data before the carrier system reset is asserted to the module.

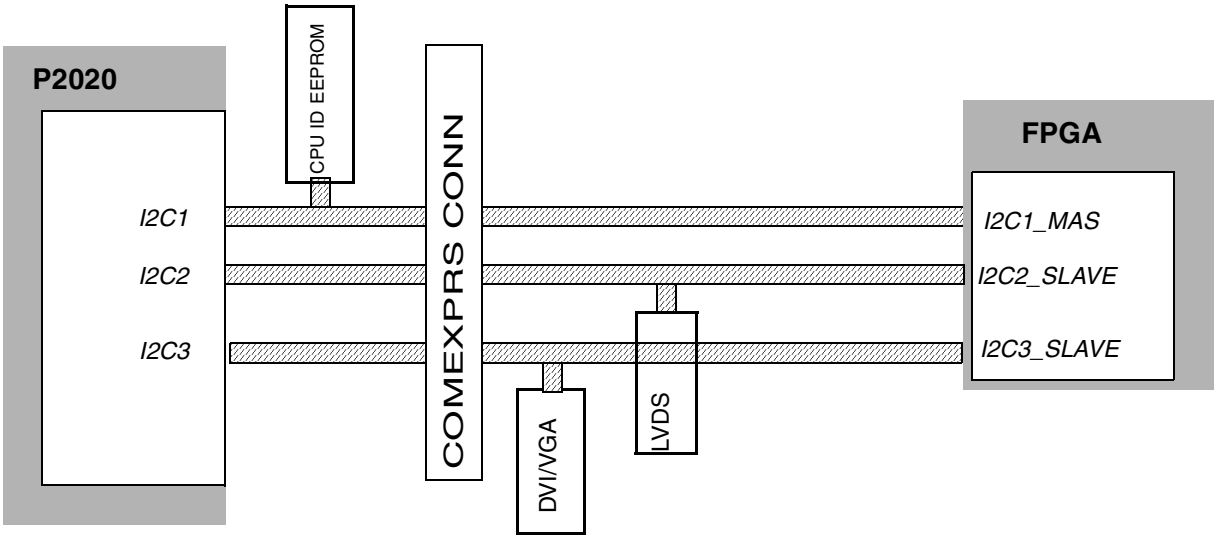


Figure 32. P2020 I²C Connectivity to Carrier Board FPGA

I²C bus device addresses are summarized in Table 21.

Table 21. P2020 I²C Bus Device Map

I²C Bus	I²C Address	Device	Notes
1	0x21	Reserved	—
1	0x22	Reserved	—
1	0x23	IO Expander Philips PCA9555PW	Not used for P2020 module. Reserved.
1	0x34	CODEC Wolfson WM8776SEFT	Not used for P2020 COMe module. Reserved.
1	0x57	I²C slave port	Not used for P2020 COMe module. Reserved.
1	0x58	USB HUB2	On P2020 COMe module.
1	0xA0	4-Kbyte EEPROM Atmel AT24C02C or equivalent	Boot configuration I²C EEPROM on P2020 COMe module
1	0xA4	Remote I²C IO Expander Philips PCA9672PW Device ID	On carrier. Read only. See datasheet for programming instructions
1	0xA8	4-Kbyte EEPROM Atmel AT24C64A or equivalent	Stores 256 bytes of processor type data. Write protectable.
1	0xE0	I²C MUX Philips PCA9545APW	On P2020 COMe module.

Table 21. P2020 I²C Bus Device Map (continued)

I²C Bus	I²C Address	Device	Notes
2	0x36 0x66 0xA6	DDR3 devices	On P2020 COMe module
2	0x58	USB HUB1	On P2020 COMe module
2	0x60	6-bit DAC Maxim MAX5362LEUK	Not used for P2020 module. Reserved.
2	0x90	Thermal sensor National Semiconductor LM75CIM-3	On P2020 COMe module
2	0xD0	RTC	On P2020 COMe module
3	contact vendor	VGA chip VOLARI Z11M	On P2020 COMe module. Contact vendor for datasheet and see P2020 COMe module User Guide for more details.

Note: These addresses do not include the position of the LSB of the transmitted address (the read/write bit).

See Section 4, "Programming Model," for I²C implementation information.

3.3.15 Carrier Board Use of P2020 EM1 and EM2 Management Buses

The carrier board has the following types of buses:

- SGMII and RGMII PHY management
- XAUI PHY management—not applicable for P2020

Because one set of buses must span across multiple devices on the carrier board, multiplexers are used to route from the P2020 to each PHY, and switches are used to control these multiplexers.

PHY management bus control is summarized in Table 22 and Table 23.

Table 22. P2020 PHY Management Bus Map for EMI1 on Carrier Board

Bus	SW4[3:4]	Device
EMI1	00	On board RGMI PHYI
EMI1	01	Slot 2 SGMII
EMI1	10	Slot 3 SGMII

Table 23. P2020 PHY Management Bus Map for EMI2 on Carrier Board

Bus	SW8[4:5]	Device
EMI2	00	No Device
EMI2	01	No Device
EMI2	10	No Device
EMI2	11	Slot 3 XAUI—not applicable for P2020

3.3.16 Carrier Board Use of P2020 Debug Features

The carrier board provides a JTAG COP header and AURORA test points for debug purpose using the CodeWarrior USBTAP already installed in the system.

To upgrade the U-Boot stored on the COMe module's NOR FLASH, use the CodeWarrior USBTAP tool. See the *COMX-P2020 COM Express Module* installation and user manual and the *Mentor Embedded Linux for Freescale COMe P2020 System Builder Quick Start Guide* for more details.

3.3.17 Carrier Board Clock Generation from P2020 COMe2 Module Board

The carrier board clock signals are generated by the COMe module board in use. Table 24 lists the requirements of the carrier board clock signals when the carrier board is populated with a P2020 COMe2 module. For more details on the P2020 COMe2 module, see the *COMX-P2020 COM Express Module* installation and user manual.

Table 24. Carrier Board Clock Requirements When Used with P2020 COMe2 Module

COMe2 Clock Signal	Corresponding Carrier Board Clock Signal	Clock Frequency	Type
SD1 REFCLK	P2020 SD_REFCLK1(p,n) SLOT1 REFCLK(p,n) SLOT2 REFCLK(p,n) SLOT4 REFCLK(p,n) SLOT5 REFCLK(p,n)	100 MHz	LVDS
SD2 REFCLK	P2020 SD_REFCLK2(p,n) SLOT1 REFCLK(p,n)	100 MHz	LVDS

Figure 33 shows the principal clock connections from the P2020 COMe2 module to the carrier board.

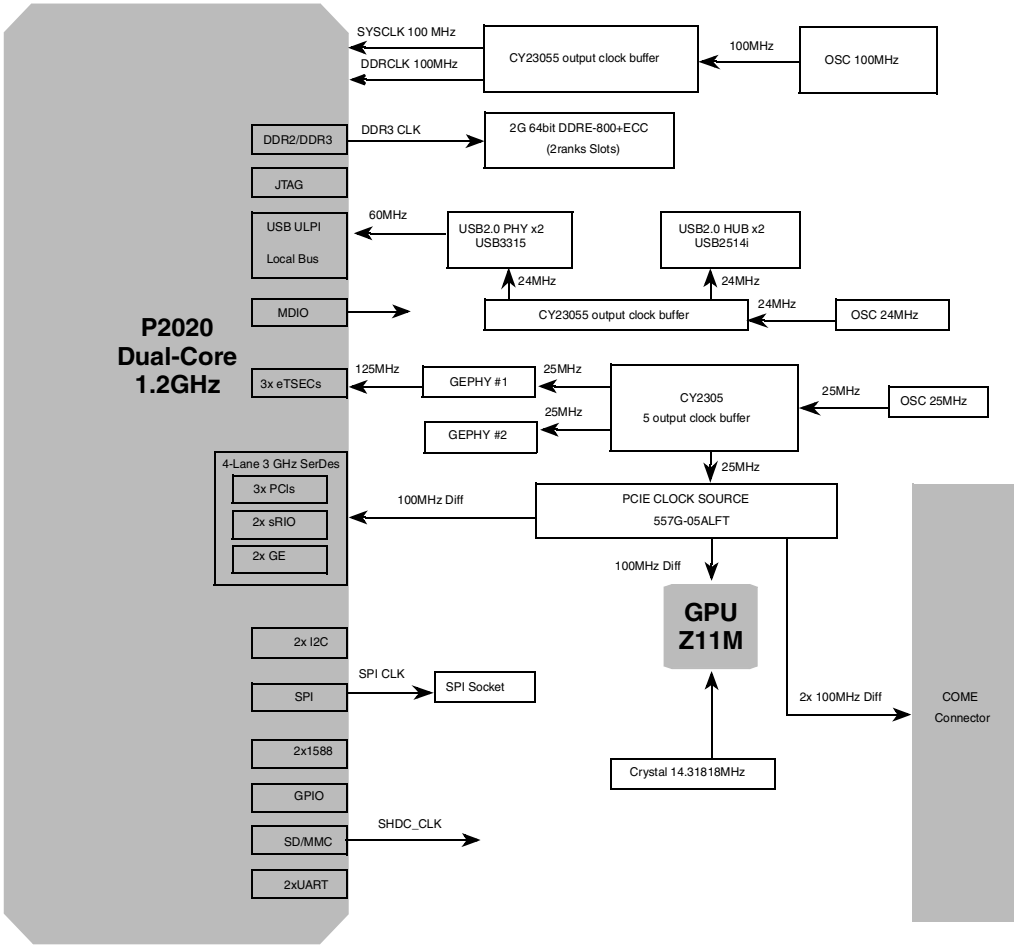


Figure 33. P2020 COMe1 Module Clock Architecture

Conversely, the carrier board provides a battery to the RTC clock to keep time while the system is turned off as shown in Table 25.

Table 25. P2020 Clock Connections to Carrier Board

Pin Count	Signal Names	Connections
1	RTC	Arbitrary timebase frequency
11	Total pins in this group	

NOTE

The SerDes and Ethernet clocks are included in their respective sections.

3.3.18 P2020 Power

An ATX power supply (600 W) is provided in the system to support the P2020 COMe1 module and all its I/O cards. VCC_12, VCC_5V_STBY, VCC_RTC_BAT are provided to the COMe module from the carrier board.

4 Programming Model

For I^2C master reading of the processor ID EEPROM, see *ProcessorID Format for Power Architecture® Development Systems*.

Table 26 describes the EEPROM on the COMe module at address 0xA8 supplying the processor ID and other attributes. The ProcessorID device is implemented by a 256-byte serial I^2C EEPROM. A typical device is the Atmel AT24C02 or equivalent.

Table 26. ProcessorID EEPROM Data Requirements

Characteristic	Value
Size	256 bytes[1]
Address	0xA8
Addressing	Non-extended
I^2C bus	I^2C21
Write protection	Required

[1] Maximum size for non-extended addressing

4.1 I^2C Slave Format

The I2C1 bus is used to drive the I^2C expander on the COMe carrier board. Figure 34 shows the mapping of FPGA_GPIO and IXATT_GPIO0 signals that are used to select QUICC Engine multiplexers and functions via software.

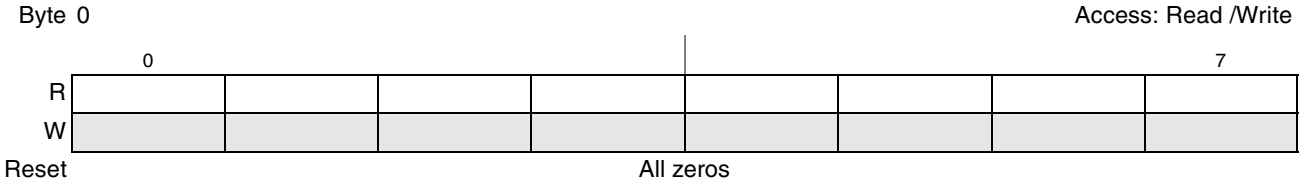


Figure 34. I^2C Slave Byte Signal Mapping

Table 27. i^2C Byte Field Descriptions

Bits	Signals
0	IXATT_GPIO0
1	FPGA_GPIO4
2	IXXAT_GPIO2

Table 27. i²C Byte Field Descriptions (continued)

Bits	Signals
3	IXXAT_GPIO3
4	FPGA_GPIO0
5	FPGA_GPIO1
6	FPGA_GPIO2
7	FPGA_GPIO3

5 Revision History

Table 28 provides a revision history for this design workbook.

Table 28. Document Revision History

Rev. Number	Date	Substantive Change(s)
1	02/2011	In the second paragraph, changed the definition of “SBC” to be “single-board computing.”
0	01/2011	Initial public release

Appendix A References

Table A-1 lists useful documentation references.

Table A-1. Useful References

Topic	Document Title	Document ID
System design	*P4080 QorIQ Integrated Processor Hardware Specifications*	P4080EC
	P2020 QorIQ Integrated Processor Hardware Specifications	P2020EC
SoC programming	*P4080 QorIQ Integrated Multicore Communication Processor Family Reference Manual*	P4080RM
	P2020 QorIQ Integrated Multicore Communication Processor Family Reference Manual	P2020RM
Switch configuration	P4080DS Configuration Sheet	—
	P2020DS Configuration Sheet	—
SystemID format	*The SystemID Format for Power Architecture® Development Systems*	AN3638

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